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# OPTIMIZATION OF SIMPLE COMBINATIONAL UNIVERSAL LOGIC GATES

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## ABSTRACT

In this paper we have develop the optimization of simple combinational universal logic gates optimized by Minitab19. The model of an optimized logic circuit that outfits a preferred Boolean utility is interest. We don't forget fast transformation of a multilevel and multioutput circuit with AND, OR and NOT gates into a functionally equal circuit with NAND and NOR gates. The venture may be solved via changing AND and OR gates through NAND or NOR gates, which requires in a few cases introducing the extra inverters or splitting the gates. That is, the conduct of such a circuit may be defined through the combination of a functional and timing specification derived from the circuit topology and the element specifications. The traditional gate minimization strategies produce simplified expressions in the trendy bureaucracy: sum of products (SOP) or product of sums (POS). The SOP shape may be transformed to a NAND expression through a regular, but the transformation does not result in optimized circuit; neither in terms of the range of gates, nor the range of level. The results predicted by the developed model are concurring well within the measured values in Response surface method by minitab19. Pearson correlation of logic circuit I/P and logic circuit O/P is 1.000. Experimental effects show our technique produces better consequences compared to remodeling the SOP form to the NAND expression, with admire to the variety of expected mean square logic circuit O/P value is 1.00 (2) + 3.70 (1) and transistors of the logic circuit.

**Keywords:** Universal Logic Gates, Boolean Operations, Optimization, Minitab19, SOP & POS, Response Surface Method.

## I. INTRODUCTION

In this paper us optimization of all the simple combinational logic gates, along with we use Boolean algebra to clarify and examine circuits with the intention of combinational of logic gates. These circuits may be classified as combinational logic circuit due to the fact, by several times; the logic stage at the output relies upon scheduled the combination of universal logic level current at the input. A combinational circuit has no reminiscence distinctive, so their outputs depend most effective on the present assessment of its inputs.

To start, we are able to go similarly addicted to the oversimplification of universal logic circuits. Two methods could be used: one makes utilize of Boolean algebra theorem; the alternative uses a mapping method. In adding together, we determination have an optimized at simple strategies for designing combinational universal logic circuits to assure a specified set of necessities. A complete optimized of universal logic-circuit design is not considered one of our objectives, but the methods we introduce will offer an amazing creation to good judgment design.

## II. UNIVERSAL GATES

A universal gate is a gate that may apply any Boolean operation not including want to apply some other gate type. In practice, this is positive seeing that NAND and NOR gates are budget friendly and less difficult to fabricate and are the simple gates used in all IC digital logic families.

The NAND gate and nor gate are universal gate because its repeated use can produce other logic gates. The table underneath show how NAND gates may be linked to produce inverter (i.e., NOT gate) AND gate and OR gate.

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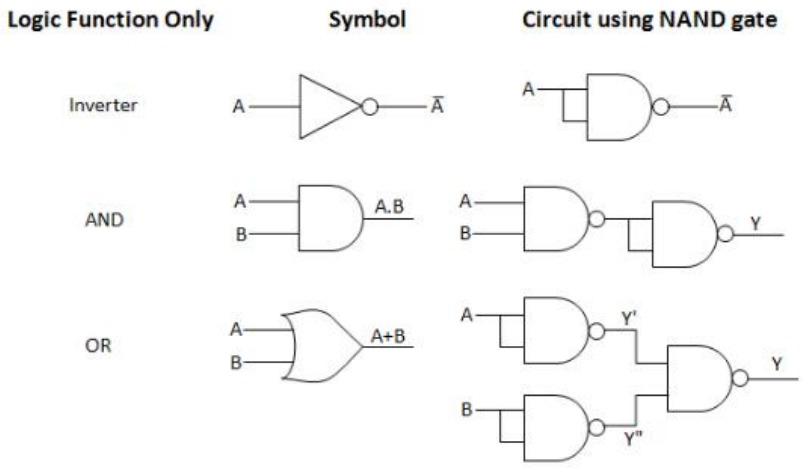


**Fig.1** Universal Logic Gates and Complete Sets

### 2.1 NOT gate from NAND gates

When two inputs to NAND gate are joined to accumulate so that has one input, the ensuing circuit is NOT gate. The truth table also displays this reality.

**Table 1:** NOT gate from NAND gate truth table

| A | BC = A | Y |
|---|---|---|
| 0 | 0 | 1 |
| 1 | 1 | 0 |

### 2.2 AND gate from NAND gates

For this reason, we use gates in a way as shown above. The output of first NAND gate is given to the second one NAND gate. Acting as inverter (i.e., inputs of NAND gate joined) the resulting circuit is the AND gate. The output Y' of first NAND gate (AND gate observed by NOT gate) is inverted output of AND gate. The second NAND gate performing as inverter auxiliary inverts it so that the extremely last output Y is that of AND gate truth table also displays this reality.

**Table 2:** AND gate from NAND gate with truth table

| A | B | Y' | Y |
|---|---|---|---|
| 0 | 0 | 1 | 0 |
| 0 | 1 | 1 | 0 |
| 1 | 0 | 1 | 0 |
| 1 | 1 | 0 | 1 |

### 2.3 OR gate from NAND gates

For this reason, we use three NAND gates in a manner as proven above. The first two NAND gates are operated as NOT gates and their output are fed to the third. The resulting circuit is OR gate. The truth table also displays this reality.

**Table 3:** OR gate from NAND gates with truth table

| A | B | Y' = $\bar{A}$ | Y"=$\bar{B}$ | Y |
|---|---|---|---|---|
| 0 | 0 | 1 | 1 | 0 |
| 0 | 1 | 1 | 0 | 1 |
| 1 | 0 | 0 | 1 | 1 |
| 1 | 1 | 0 | 0 | 1 |

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## III. LOGIC FUNCTIONS USING UNIVERSAL GATES

### 3.1 Equipments along with components essential

- ICs – 7400, 7408, 7402, 7486, 7432.
- Multimeter, CRO probes and CRO.
- IC trainer equipment and patch chords.

### 3.1.1 Digital Logic IC's

- 7408: Quad key in AND
- 7400: Quad key in NAND
- Gates 7404: Hex inverters
- Gates 7432: Quad key in OR
- Gates 7486: Quad key in XOR
- Gates 7402: Quad key in NOR

### 3.2 Universality of NAND ad NOR gates

### 3.2.1 Basic logic functions using NAND gates

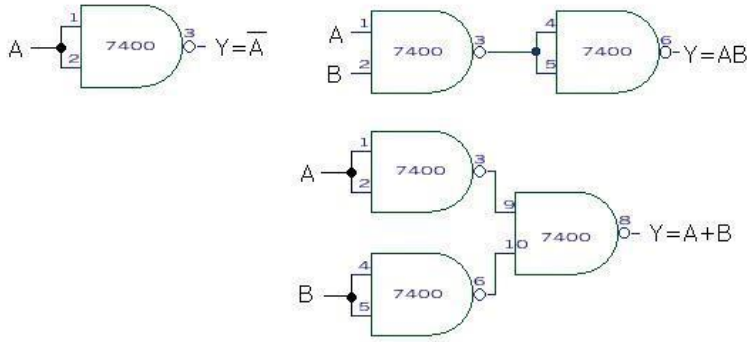


**Fig.2** Basic logic functions using NAND gates

### 3.2.2 Basic logic functions using NOR gates

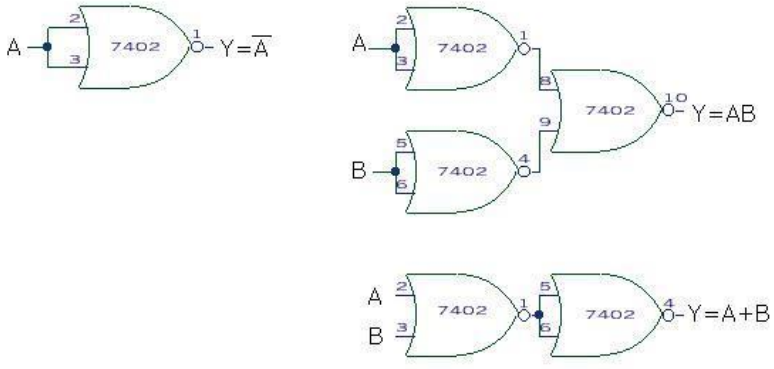


**Fig.3** Basic logic functions using NOR gates

### 3.3 Assembly of Combinational Circuits

Design a logic circuit among 4 inputs A,B,C,D that will generate output '1' only each time two bordering input variables are 1's. A and D must also be treated as bordering. Apply it by universal logic.

**Table 4:** Truth Tables for Combinational Circuits

| INPUT | | | | OUTPUT |
|---|---|---|---|---|
| A | B | C | D | F |
| 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 0 | 1 | 0 |

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| | | | | |
|---|---|---|---|---|
| 0 | 0 | 1 | 0 | 0 |
| 0 | 0 | 1 | 1 | 1 |
| 0 | 1 | 0 | 0 | 0 |
| 0 | 1 | 0 | 1 | 0 |
| 0 | 1 | 1 | 0 | 1 |
| 0 | 1 | 1 | 1 | 1 |
| 1 | 0 | 0 | 0 | 0 |
| 1 | 0 | 0 | 1 | 1 |
| 1 | 0 | 1 | 0 | 0 |
| 1 | 0 | 1 | 1 | 1 |
| 1 | 1 | 0 | 0 | 1 |
| 1 | 1 | 0 | 1 | 1 |
| 1 | 1 | 1 | 0 | 1 |
| 1 | 1 | 1 | 1 | 1 |

## IV. OPTIMAL DESIGN

Design a logic circuit among Response surface design selected according to D-optimality

- Number of candidate design points: 14
- Number of design points in optimal design: 20
- Model terms: Block, A, B, AA, BB, AB

**Table 5:** Optimal table for Combinational Circuits

| S.L NO | PTTYPE | BLOCKS | LOGIC CIRCUIT I/P | LOGIC CIRCUIT O/P |
|---|---|---|---|---|
| 1. | -1 | 2 | 0.50000 | 0.50000 |
| 2. | -1 | 2 | -0.20711 | -0.20711 |
| 3. | 1 | 1 | 1.00000 | 1.00000 |
| 4. | -1 | 2 | 0.50000 | 0.50000 |
| 5. | -1 | 2 | 1.20711 | 1.20711 |
| 6. | 1 | 1 | 0.00000 | 0.00000 |
| 7. | 0 | 1 | 0.50000 | 0.50000 |
| 8. | 1 | 1 | 0.00000 | 0.00000 |
| 9. | 1 | 1 | 1.00000 | 1.00000 |
| 10. | 0 | 2 | 0.50000 | 0.50000 |
| 11. | 1 | 1 | 0.00000 | 0.00000 |
| 12. | 1 | 1 | 0.00000 | 0.00000 |
| 13. | -1 | 2 | 1.20711 | 1.20711 |
| 14. | -1 | 2 | 0.50000 | 0.50000 |
| 15. | 1 | 1 | 1.00000 | 1.00000 |
| 16. | 1 | 1 | 1.00000 | 1.00000 |
| 17. | -1 | 2 | 0.50000 | 0.50000 |
| 18. | -1 | 2 | -0.20711 | -0.20711 |
| 19. | 0 | 1 | 0.50000 | 0.50000 |
| 20. | 0 | 2 | 0.50000 | 0.50000 |

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### 4.1 Optimal Design Parameters

| | |
|---|---|
| Condition number: | 2.5 |
| D-optimality (determinant of XTX): | 83886080 |
| A-optimality (trace of inv(XTX)): | 0.76875 |
| G-optimality (avg leverage/max leverage): | 0.965517 |
| V-optimality (average leverage): | 0.35 |
| Maximum leverage: | 0.3625 |

## V. RESULTS AND DISCUSSION

### 5.1 Mood's median test

When comparing the common of two or further groups with the assist of hypothesis tests, the assumption is that the statistics is a pattern from a typically distributed population. That is why speculation tests which includes the t-take a look at, paired t-check and analysis of variation (ANOVA) are also known as parametric tests.

The Mood's median take a look at is a nonparametric test that is used to test the equality of medians from or further populations. Therefore, it provides a nonparametric alternative to the only-way ANOVA. The Mood's test works once the Y variable is constant, discrete-ordinal or discrete-be counted, and the X variable is discrete among two or further attributes.

**Table 6:** Descriptive Statistics

| logic circuit O/P | Median | N <= Overall Median | N > Overall Median | Q3 – Q1 | 95% Median CI |
|---|---|---|---|---|---|
| -0.20711 | -0.20711 | 2 | 0 | * | (-0.207107, -0.207107) |
| 0.00000 | 0.00000 | 4 | 0 | 0 | (0, 0) |
| 0.50000 | 0.50000 | 8 | 0 | 0 | (0.5, 0.5) |
| 1.00000 | 1.00000 | 0 | 4 | 0 | (1, 1) |
| 1.20711 | 1.20711 | 0 | 2 | * | (1.20711, 1.20711) |
| Overall | 0.50000 | | | | |

Levels with < 6 observations have confidence < 95.0%

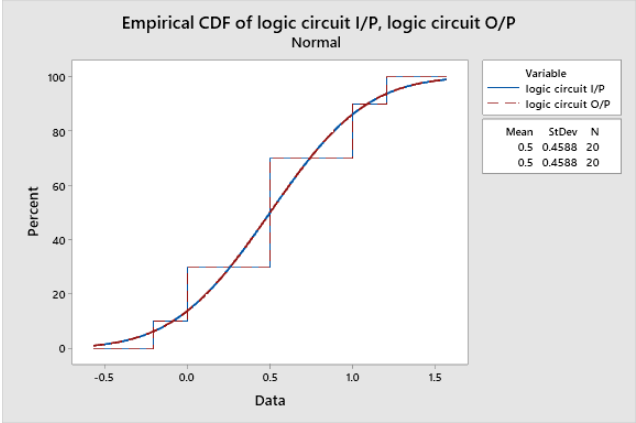


**Fig.4** Empirical logic circuit

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**Table 7:** Total Statistics

| Variable | Total Count | Mean | StDev |
|---|---|---|---|
| logic circuit I/P | 20 | 0.5000 | 0.4588 |
| logic circuit O/P | 20 | 0.5000 | 0.4588 |
| Total | 20 | 1.0000 | 0.9177 |

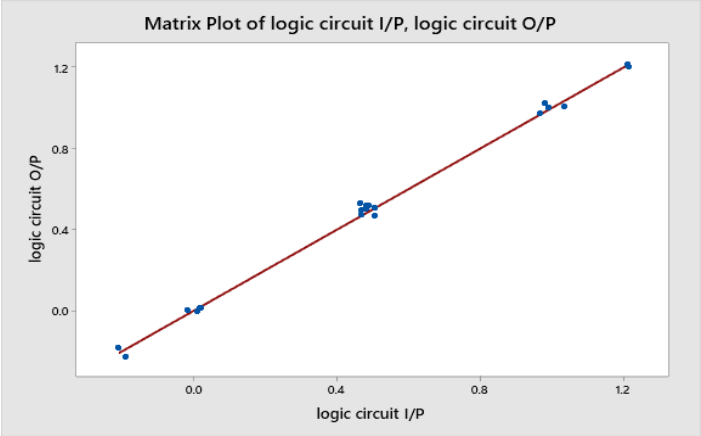


**Fig.5** Item Analysis of logic circuit I/P, logic circuit O/P

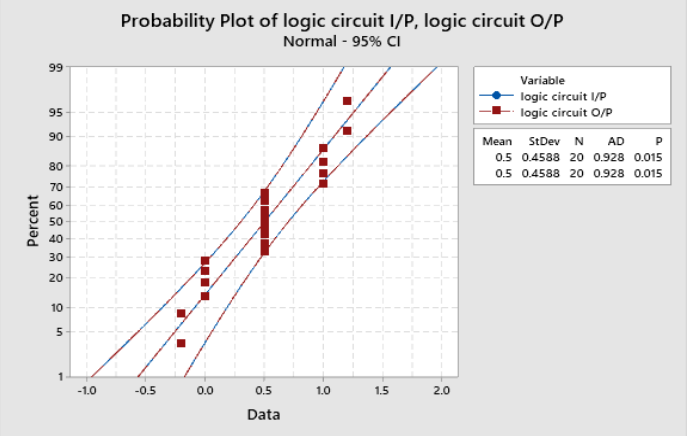


**Fig.6** Probability Plot of logic circuits

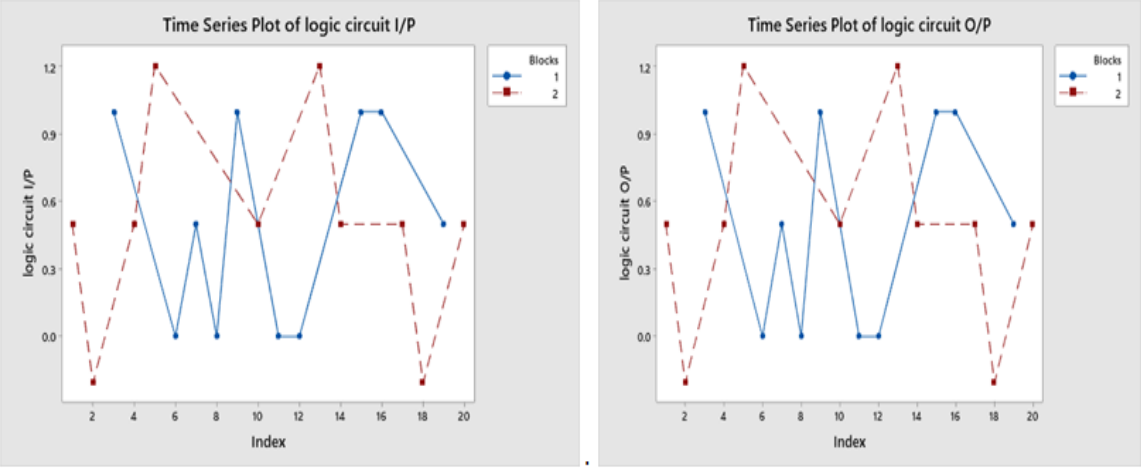


**Fig.7** Time series plot of logic circuits

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**Table 8**

| SL.NO | CIRCUIT | VARIABLE |
|---|---|---|
| 1. | logic circuit O/P | 1.00 (2) + 3.70 (1) |
| 2. | Error | 1.00 (2) |

## VI. CONCLUSION

We have exposed a genetic encoding method for the synthesis of combinational logic universal circuits. In its place of typically worn set of gates, i.e. AND, OR, NOT, XOR we worn the universal logic NAND gates. First we worn two-input NAND gates and intended to optimize the circuit primarily based on the range of gates and levels. Then we had worn multiple input NAND gates to obtain a circuit with an optimized variety of transistors. The experimental results demonstrated that our approach of expected mean square logic circuit O/P value is 1.00 (2) + 3.70 (1) and transistors of the logic circuit.

## VII. REFERENCES

[1] McCluskey, E.J.: Minimization of Boolean function.
[2] Katz, R.H., Borriello, G.: Contemporary logic design. Prentice-Hall, Englewood Cliffs (2004)
[3] Chong, K.H., Aris, I.B., Bashi, S.M.: Application of evolutionary algorithm in optimization digital structure design. AIML Journal 6 (2006)
[4] Melanie, M.: An Introduction to genetic algorithms. The MIT Press, Cambridge (1999)
[5] C.A., Christiansen, Coello, A.D. Aguirre, A.H.: Automated design of combinational logic circuit using genetic algorithms. In: Int. Conf. on Artificial Neural Nets and Genetic Algorithms, pp. 335–338 (1997)
[6] G. E. Moore, "Gramming supplementary components onto integrated circuit," Electronics, vol. 38, pp. 114-117, 1965.
[7] C. Paar. Optimized arithmetic for Reed-Solomon encoders. In IEEE
[8] W. Eerenstein, N. D. Mathur, and J. F. Scott, "Multiferroic and magnetoelectric materials,"
[9] Khitun, D. E. Nikonov, M. Bao, K. Galatsis, and K. L. Wang, "Efficiency of spin-wave bus for information transmission," IEEE Transactions on Electron Devices, vol. 54, pp. 3418-21, 2007.
[10] H. Jackson and D. Hodges psychoanalysis and devise of Digital Integrated Circuits, McGraw-Hill, 1988
[11] Horowitz, E., Sahni, S. Fundamentals of data structures. W H Freeman & Co (Sd), New York (1983) Weste, N.H.E Eshraghian.
[12] Veendrick, “Short-Circuit indulgence of fixed CMOS Circuitry and Its collision on the devise of Buffer Circuits,” IEEE