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A REVIEW ON LOW-NOISE AMPLIFIER

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ABSTRACT

In this paper a review on LNA is presented and different techniques have been discussed for designing the LNA. Cascode amplifier technique is used to increase the bandwidth and it is used for high voltage application. Gainboosting technique is used to boost the gain of the amplifier; Low power dissipation can be achieved by using current reuse technique. Size of the designed chip should be as minimum as possible with not compromising in speed of the operation so for this memrister based tunable inductor LNA was used to reduce the chip size with good speed. Re-configurable LNAs are most popular because they can work on different frequencies with the same circuit.

Keywords: Cascode, Gain-Boosting, Current Reuse, Memrister, Re-configurable LNA.

I.

INTRODUCTION

We are surrounded by the IoT devices and the communication between them has become smoother with time. Each device consists of receiver system within it and for maintaining the healthy communication between devices receiver should be well optimized. For better speed of a device the chip area should be as minimum as possible and the reduced size also reduced the cost of the device. An important role has been played by low-noise amplifier in the overall performance of receivers since they are used as first active device after the antenna stage. LNA must provide high gain, low noise figure (NF), and good input matching for multiple frequency bands.

Band switching and gain switching in LNAs usually require multiple switchable amplification transistors, capacitors, and inductors to achieve the desired re-configurability [2].For reducing the chip size an LNA is proposed which is operating at two distinct frequencies 2.4-5.2 GHz and for further reducing the chip size memristor based LNA was proposed [1]-[2]. Power dissipation and gain for any device played an important with the advancement in technology and for better battery performance of a device and in terms of gain LNA should be designed with current reuse, gm-boosting and sub-threshlod techniques [3]-[4]. Through transmitter sender sends a signal which is to be communicated and at the receiver end this signal is received by the receiver and the signals which are received are the radio signals.



Fig 1: Transmitter and Receiver System

Radio signals are received by the receiver but while travelling from antenna and through the channel the transmitted signal will attenuate and at the receiver end we will receive a very low amplitude signal. This low amplitude signal will have to be amplified so that the receiver can detect the transmitted signal accurately. In any



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communication system receiver plays an important role because it decides the quality of the signal which was transmitted by the the transmitter. Receiver system contains many components like LNA, Demodulator, IF Stage, Detector, etc. But in all these components LNA is the first active device which directly receive the attenuated signal after the receiver antenna stage. As the users are increasing and so the demand of the different devices are also increasing. For fulfillment of the user's demand more High power, Higher bandwidth and Highly sensitive devices are required.

II. METHODOLOGY

There are different techniques available for designing the LNA circuit for better reciever response. Some important and mostly used techniques are discussed with the circuit that were proposed with that techniques.

1. Dual Band Re-configurable LNA:

The below LNA circuit was operated at 2.4 and 5.2 GHz bands, This type of circuits called as re-configurable LNAs because a single circuit works on two different frequencies. All the NMOS based switches are considered to be open when the circuit is operating at 5.2 GHz frequency [1]. In this case, Transistor biasing to the M1A is proved through R1 from VB1 and M1A is acting as a input transistor.



Fig 2: Dual Band Re-Configurable LNA Circuit [1]

Where, g_{m1A} and C_{gs1A} are the transconductance and the gate capacitance of M_{1A}, respectively, and \mathcal{O}_H is the operating frequency at this band. A parallel connection is situated between the transistors M_{1A} and M_{1B}[1] When the circuit is operating at 2.4 GHz frequency. Output impedance is matched by using to 500hm by the shunt inductor L_D and the series capacitor C_{1A}. In this case the bias voltage to M_{1A} and M_{1B} is provided by (R_{2VB1} + R_{1Vb2})/(R₁ + R₂) through R₁ and R₂. When the LNA circuit is operated at low frequency band, the output impedance of 500hm is provided by capacitor c_{1B} and C₂ network by the switches SW₂ to SW₃.

2. Memristor based tunable inductor LNA:

Maximum performance has been shown by memristor devices and also these devices takes less space on the chip. . The integrated spiral inductors could be tuned with the help of memristive device [2]. For achieving reconfigurable LNA the below figure is showing a dual band cascode common source with inductive degeneration [2] with an integrated spiral inductors that could be turned on with memristor based devices. The resistance of the nonvolatile memories like RAM, CBRAM and Phase Change Memory (PCM) rely on the previous values of voltage and currents change, and kept whenever the external change is no longer available. These devices can be used as a



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switch and memory storage elements with a high resistive state (HRS, ROFF) and a low resistive state (LRS, RON) [2] due to the property of high non-linearity of these devices. Roff is called reset when switching from Ron to Roff and the reverse of this is called se.. In the below circuit the gate inductor (L_G) and the output inductor (L_{out}) are memristor-based tunable inductors. The input impedance of this circuit is given by

$$Z_{in} \approx \frac{1}{j\omega C_{gs1}} + j\omega (L_s + L_G) + \frac{g_m L_s}{C_{gs1}}$$
(1)



Fig 3: LNA using memristor based tunable inductor [2]

For resonating at the desired frequency an inductor LG is added with the capacitance CGS1, eliminating the undesired reactance. For matching the output, Inductor Lout resonate with capacitor Cout1 and the bank of Cout2. Transistor M2 is cascaded to reduce the miller effect of gate-drain transistor Cgd of M1. A current mirror is formed between transistor M3 and M1 for providing a operating point. For matching the LNA for different frequencies variable inductors LG and Lout are used. Inductor LG varies with two inductor values to resonate Cgs1 at both frequencies [2].

3. Low Power re-configurable LNA:

It is always necessary to have a device with better battery life. So it is recommended to pick the LNA circuits which dissipate less power while in use. For wireless communication and IoT applications ultra low power LNAs are required but the power of LNA is reported in mW. By employing current-reused, forward-body-bias techniques [7], and an inductorless LNA with triple cross-coupling technique is also durable. In triple cross-coupling technique the subthreshold region of MOS transistor is a key factor [5]. In order to make the device work in low power status, MOSFET's must work in the low current or/and low voltage region. As it is true that when VGs is less than one threshold then MOSFET is considered to be turned off means there is no current is flowing from drain to source. When VGs is equal to one threshold then there is a 'weak' inversion layer still exists and some current flows from drain to source. Even VGs is less than one threshold there is a finite drain current ID.



International Research Journal ofModernization in EngineeringTechnology and ScienceVolume:03/Issue:06/June-2021Impact Factor- 5.354www.irjmets.com





The circuit consisted of Common Gate(CG) topology as this topology provides higher Bandwidth(BW), Linearity and stability factor but at the same time it also decreases gain and increase the noise figure compared to Common Source (CS) LNA. To improve the gain with CG gain-boosting technique can be employed. With use of active devices the noise and stability performance goes down so to improve this situation passive devices (transformer feedback) is used[7]. For lowering the power dissipation in the circuit current reuse and forward-body-bias technique were used[7]. The circuit operated at 0:63V supply voltage and exhibits low power dissipation with significant gain by using forward body- bias in Gm-boosted CG input stage.

4. Ultra Low Power LNA:

When $V_{gs} < V_{th}$ then the NMOS transistor is considered to worked in cut off region. In fact, when Vgs equals to V_{th}, a weak inversion layer still exists and some current flows from drain to source. In this case current depends on V_{gs}. So when compared with saturation region much power will be saved [5].



Fig 5: An ultra low power LNA [5]

The circuit provides less G_m and f_T than saturation region and that's why it produces less gain. To achieve low power consumption the combination of a fold cascode type and subthreshold was used and to solve the problem of low gain cascode topology was employed.

III. RESULTS AND DISCUSSION

The below table is showing a comparison of different results based on the reported LNAs in reviews.



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Table 1. Comparison of reported LNAs							
Technology	Frequency	S ₂₁ (dB)	S ₂₂ (dB)	S ₁₁	Noise	Power	FOM
	(GHz)			(dB)	Figure	(mW)	
[1] 0.18um	2.4/5.2	10.1/10.9	-10.5/-17	-10.1/-	2.9/3.7	11.7/5.7	
				11			
[2] 0.18um	3/10	19.8	-9.2	-10.6	3.4	14.8	4.73
[3] 0.18um	1.86/2.4	9.68/10.17			5.34/3.77	1.61	
[4] 0.18um	0.4-1	17	-18		4.2	0.2	63.34
[5] 0.18um	3-10	19.8	-11	-11	3.4	14.8	4.73
[6] 0.45um	2.4	14.1	-9.4	-7.5	2.4-2.9	7.7	

IV. CONCLUSION

A review is done on LNA and compared the different results based on the circuit proposed. For low power dissipation cross coupling, current reuse and common gate cascode topology are considered better in comparison with other techniques while in terms of better gain, LNA with CMOS distributed amplifier and cascode stage inductively degenerated technique is considered. For maintaining the chip area switched capacitors and inductors technique is used and for further reducing the chip size memristor based LNA is proposed. LNA circuits are designed on different technology like 45nm, 69nm, 130nm, 180nm, etc. LNA is used in many devices like Wi-Fi, Bluetooth, IoT and many more.

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International Research Journal of
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