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A REVIEW ON SPECIAL MEMORY ARCHITECTURES

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ABSTRACT

Memory architectures are fundamental components in computing systems, playing a critical role in storing and accessing data. This review paper provides an overview of various memory architectures with a highlight on hybrid and concurrent memory architectures, ranging from traditional Static Random-Access Memory (SRAM) and Dynamic Random-Access Memory (DRAM) to emerging technologies such as Non-Volatile Memory (NVM) and 3D-stacked memories. The characteristics, advantages, and limitations of each architecture is explored, highlighting their suitability for different applications. Additionally, recent advancements, challenges, and future trends in memory design are discussed, including the integration of novel materials and device structures, neuromorphic computing, and in-memory computing paradigms. Understanding the diverse landscape of memory architectures is essential for designing efficient and scalable computing systems to meet the growing demands of modern applications and technologies.

Keywords: Special Memory Architectures, Hybrid Memory, Concurrency.

I. INTRODUCTION

Semiconductor memory, particularly Random Access Memory (RAM), stands as a cornerstone in the realm of computing, providing swift and temporary data storage crucial for the seamless operation of electronic devices. RAM's fundamental role lies in facilitating rapid access to data, enabling processors to quickly retrieve and manipulate information during active tasks. Unlike permanent storage solutions such as hard drives, RAM offers high-speed access to data, contributing directly to the responsiveness and overall performance of computing systems. As a pivotal component in modern electronic devices, semiconductor memory RAM plays a pivotal role in shaping the efficiency and responsiveness of computing experiences. The area efficiency of the memory array, i.e., the number of stored data bits per unit area, is one of the key design criteria that determine the overall storage capacity and, hence, the memory cost per bit. Another important issue is the memory access time, i.e., the time required to store and/or retrieve a particular data bit in the memory array. The access time determines the memory speed, which is an important performance criterion of the memory array. Finally, the static and dynamic power consumption of the memory array is a significant factor to be considered in the design, because of the increasing importance of low-power applications.

Hybrid memory architectures have emerged as promising solutions to address the growing demands for memory systems in VLSI (Very Large Scale Integration) designs. These architectures combine the strengths of different memory technologies, such as SRAM (Static Random-Access Memory), DRAM (Dynamic Random-Access Memory), and emerging non-volatile memory (NVM) technologies like PCM (Phase-Change Memory) and ReRAM (Resistive Random-Access Memory). By integrating diverse memory types, hybrid architectures aim to optimize performance, energy efficiency, and reliability while overcoming the limitations inherent in individual memory technologies. This introduction explores the rationale behind hybrid memory architectures, their key benefits, challenges, and emerging trends in their design and implementation within VLSI systems.

High Concurrency access to a structured memory array finds widespread application in data-intensive tasks, such as table management in databases and updating weight matrices in graph applications. Traditional approaches involve sequential read and write access to multiple rows of an embedded memory array, However, in data-intensive high-concurrency memory access scenarios and also in compute-in-memory (CiM) architectures, where increased parallelism and strong computing capabilities are crucial, this sequential approach introduces significant latency, becoming a performance bottleneck. Additionally, the energy consumption per access is high with large parasitic capacitance during read and write operations.

Consequently, there is a compelling need to reconsider memory access patterns and supporting circuits to address the challenges posed by emerging high-concurrency applications. In a RAM device, when a particular

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address is selected, information is either stored in that cell or the contents therein are read out. However, simultaneous read and write operations preserving the data integrity are impossible.

II. BACKGROUND

The escalating demands of data-intensive applications have prompted a surge in exploration of diverse memory architectures. Traditional SRAM and DRAM technologies are being supplemented by emerging non-volatile memory (NVM) technologies like PCM, ReRAM, and MRAM, fostering innovation in memory design. Hybrid memory architectures, integrating SRAM, DRAM, and NVM technologies, have gained traction for their ability to balance performance, energy efficiency, and reliability through tiered storage hierarchies. Concurrent memory architectures, focusing on enabling simultaneous read and write operations within the memory subsystem, represent another avenue of innovation. By allowing memory cells to perform read and write operations concurrently, concurrent memory architectures aim to enhance system throughput and latency. This review paper aims to provide a comprehensive exploration of hybrid and concurrent memory architectures, elucidating their characteristics, advantages, challenges, and emerging trends to contribute to the advancement of memory system design in VLSI and beyond.

III. A REVIEW ON SPECIAL MEMORY ARCHITECTURES

The pursuit of optimizing memory architectures to achieve both good performance and improved energy efficiency has sparked a significant exploration of various Memory Architectures. This literature survey delves into a selection of research papers, each contributing to the evolving landscape of hybrid and concurrent access memory architectures, with a specific focus on achieving simultaneous read and write operations for enhanced system performance and efficiency.

Zhou et al.[1] proposed a sustainable low-power cache design with their work, "A novel low power hybrid cache using GC-EDRAM cells." Their evaluation of this innovative hybrid cache architecture reveals compelling benefits, including concurrent reading and writing operations. Replacing traditional SRAM cells with GC-eDRAM cells for data storage, while retaining SRAM cells for tag arrays, optimally merges strengths. The results showcase reduced energy consumption and a smaller silicon footprint, underscoring the architecture's potential for future embedded CPUs.

Furthermore, within cache operations, a write-through cache strategy is explored. This approach permits immediate reading after writing, conserving clock cycles through overlapped operations. This strategy, coupled with the hybrid architecture's concurrent capabilities, highlights the significant efficiency gains achieved by merging SRAM and DRAM technologies. This work significantly contributes to the improved cache performance and energy efficiency.

In another implementation titled FAST: A Fully-Concurrent Access SRAM Topology for High Row-wise Parallelism Applications Based on Dynamic Shift Operations by Yiming Chen et al.[2] introduces a novel fully-concurrent access SRAM topology designed to manage high-concurrency operations across multiple rows within an SRAM array. Such operations are prevalent in various applications, including conventional and emerging ones, where high parallelism is crucial, such as database table updates and parallel feature updates in graph computing. The proposed architecture utilizes a shift-based parallel access and compute approach, achieved by integrating a shifter function into each SRAM cell and creating a datapath that harnesses the high parallelism of shift operations across multiple rows. An exemplary design of a 128-row 16-column shiftable SRAM in 65nm CMOS is presented. Post-layout SPICE simulations demonstrate significant improvements in energy efficiency, with a 5.5x enhancement, and speed, with a 27.2x increase on average compared to a conventional digital near-memory computing scheme. Moreover, the design has been fabricated and tested, showing support for clock frequencies of up to 800MHz at 1.0V and 1.2GHz at 1.2V. This innovative approach to SRAM architecture offers substantial advantages in terms of energy efficiency and speed, making it well-suited for applications requiring high-concurrency operations and parallel processing capabilities. Further research and development in this area could lead to advancements in memory system design and performance, with potential implications for a wide range of computing applications.

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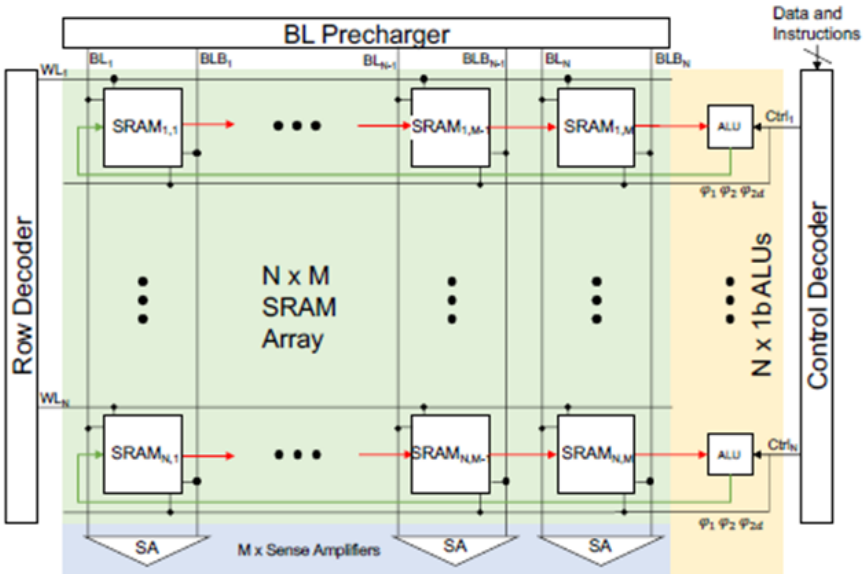

Figure 1: Shift-based in-memory computing architecture.

The paper titled "Compact 3-D-SRAM Memory With Concurrent Row and Column Data Access Capability Using Sequential Monolithic 3-D Integration" by Srinivasa et al.[6] introduces a design strategy that leverages monolithic 3D integration technology to create a two-layer 3D-SRAM cell with concurrent row and column data access capability. This innovative memory design caters to applications requiring multi-dimensional data access, offering substantial power and access time savings, and exemplifying the potential for enhanced system performance.

The work titled "Simultaneous read-write IGFET memory cell" by Hiroshi Kadota and Toyonaka[9] introduces a novel approach to random-access memory design, addressing the challenges of concurrent read and write operations. In this study, memory cells are structured with two cross-coupled inverters, each connected to distinct address and data lines to enable independent read and write operations. The architecture employs a first address line exclusively for write operations and a second address line exclusively for read operations in a column direction. Complementary data lines are utilized exclusively for write operations in a row direction, while a separate data line is reserved exclusively for read operations. Gate elements connect the complementary data lines to corresponding complementary input-output nodes within each cell, controlled by the first address line exclusively used for write operations. Additionally, the data line exclusively used for read operations is connected to one of the complementary nodes through a gate element, regulated by the data line dedicated to read operations. Complementary data lines are linked to a drive circuit responsible for delivering information to be stored, while the data line for read operations is connected to a sense amplifier. The key innovation lies in the ability to perform read and write operations simultaneously yet independently, minimizing erratic operations regardless of the timing relationships between these operations.

The work “Semiconductor Device That Enables Simultaneous Read and Write/Read Operation" by Honda et al. [10] introduces a sophisticated memory cell array with multiple cores, each serving as a unit of data erase. The design allows for the simultaneous execution of read and write/read operations by selectively choosing cores for specific actions. A notable feature is the division of cores into banks, enabling concurrent data read operations in one bank while write or erase operations are carried out in the other. This innovative approach significantly enhances the efficiency and speed of memory access, addressing the challenge of simultaneous read and write/read operations.

The work Simultaneous Read-Write Operations in Dual-Port SRAM for Flash-Based cSoCs and FPGAs introduced by Microsemi Corporation[11], extensively discusses the challenges and solutions associated with simultaneous memory access operations, particularly in the context of dual-port Static Random-Access Memory (SRAM) blocks in Microsemi SmartFusion® customizable system-on-chip (cSoC) and FPGA devices. The architecture employs two separate blocks, Block A and Block B, each with its dedicated clock signal (CLKA and CLKB). This dual-port configuration allows for both read and write operations to be independently performed

on both Block A and Block B. In particular, the focus is on how the simultaneous operations are managed in the same clock cycle at the same address in a dual-port SRAM. Different operations, such as read-write, write-write, read-read, and write-read, are examined, and the necessity for precautions to avoid data collisions is highlighted. The utilization of two separate clocks, CLK A and CLK B, plays a crucial role in controlling the timing and sequencing of read and write operations in both Block A and Block B. Proper coordination of these clock signals is essential to prevent undesired data output and ensure the integrity of simultaneous memory access operations. This resource provides valuable insights into the complexities and considerations involved in achieving simultaneous read and write operations within dual-port SRAM blocks, offering a comprehensive understanding of the role played by separate clock signals (CLKA and CLKB) in managing these operations.

The described memory array in the work by W. R. Dachtera titled Self quenching memory cell [17] presents a novel approach to memory cell design, utilizing a matrix of cells, each featuring a pair of bipolar transistor inverters. These inverters are interconnected in a cross-coupled configuration, with their collector loads connected to a first constant voltage bus, and their emitters tied together through a resistor to a second constant voltage bus. This setup allows for separate writing and reading circuits for each cell within the array, enabling simultaneous read and write operations. The innovation lies in the automatic reduction of holding current during writing, ensuring rapid switching in response to a given input switching current. This is achieved by adjusting the circuit parameters and voltage values to maintain a sufficient holding current for non-addressed cells, while automatically reducing it in the cells being accessed (read or written into). Each cell is equipped with a gated sensing circuit and at least one gated writing circuit, facilitating simultaneous reading and writing operations on the same cell.

This memory array design offers several advantages, including efficient utilization of space due to its matrix configuration, rapid switching speed enabled by automatic holding current reduction, and the ability to perform simultaneous read and write operations on individual cells. Additionally, the use of bipolar transistor inverters provides inherent robustness and reliability.

In summary, this innovative memory array architecture represents a significant advancement in memory cell design, offering improved performance and functionality compared to traditional designs. Its unique features make it well-suited for applications requiring high-speed and simultaneous read-write capabilities, potentially opening new avenues for the development of advanced computing systems.

The work by Subramani Kengeri and Jawji Chen titled Pseudo dual-port DRAM for simultaneous read/write access[14] presents a significant advancement in DRAM architecture, providing a pseudo dual-port solution for simultaneous read/write access in single-port 1-T DRAM. The invention, assigned to Altera Corp, offers potential benefits for memory-intensive applications requiring efficient and high-speed memory access capabilities.

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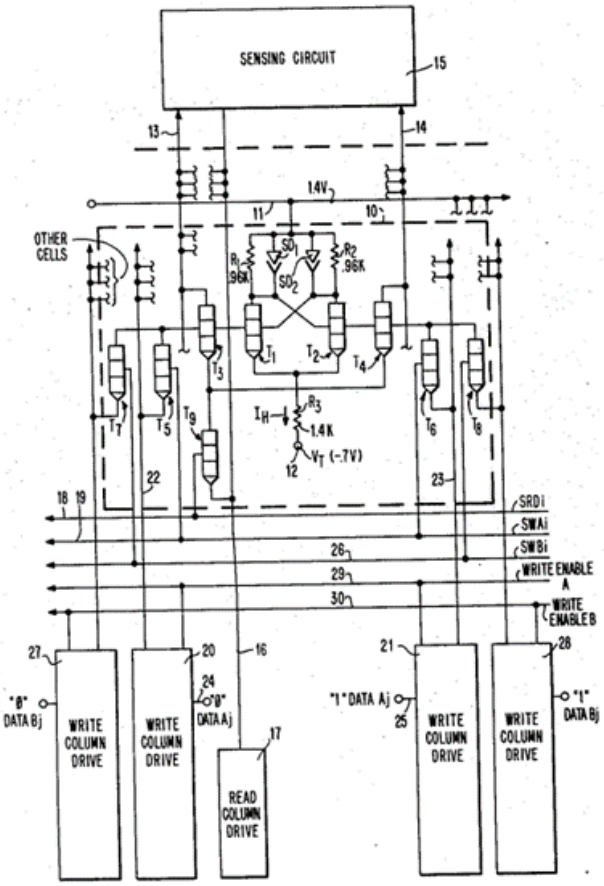

Figure 2: Self Quenching Memory Cell.

It explores a system and method for achieving simultaneous read and write access in 1-Transistor (1-T) dynamic random-access memory (DRAM) without relying on dual-port DRAM architecture. The proposed approach utilizes a single-port 1-T DRAM with a modified design of the read sense amplifier (RSA) to enable both read and write accesses within a single clock cycle. By isolating the read bitline (LBL) from the RSA during read access and enabling write data transfer during the same clock cycle, the single-port 1-T DRAM emulates the simultaneous read/write capability of dual-port memory while retaining the high performance and compact size characteristic of 1-T DRAM. The proposed method facilitates simultaneous read and write accesses in single-port 1-T DRAM by leveraging a modified RSA and access gating mechanisms. During read access, data is transferred to the RSA via the LBL, while the LBL is isolated to accommodate write data transfer. Subsequently, write data is driven onto the write global bitline (WGBL) and held, preventing it from reaching the LBL. Upon isolating the LBL from the RSA, the write pass gate is enabled, allowing the write data to enter the LBL and be written into the memory cell. This innovative approach enables seamless simultaneous read and write operations within a single clock cycle in single-port 1-T DRAM, offering enhanced memory access capabilities without the need for dual-port architecture.

In the work titled Memory device with simultaneous write and read addressed memory cells by J. E. Gersbach [16] the described memory arrangement presents a novel approach to enabling rapid data transfer between memory cells within the arrangement while reading the data. Each memory cell comprises a pair of transistors coupled between bit read lines, with a separate pair of bit read lines assigned to each column of memory cells. Additionally, each memory cell is equipped with a pair of write transistors coupled between bit write lines, with another pair of bit write lines associated with each column of cells. Read and write decoders are coupled to the rows of memory cells, allowing for orthogonal arrangement to the columns. Switching means facilitate the direct transfer of data from one memory cell to another within the arrangement while simultaneously reading the transmitted information.

In operation, when the read control circuit for one line of the arrangement and the write control circuit for a second line are activated, data retrieved from the first line of memory cells can be simultaneously transmitted

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to a second line. Write transistors are provided in parallel with the cross-coupled transistors, with emitter electrodes connected to write decoders via write word lines. The base electrodes of the write transistors are connected to switches via transistors configured as emitter followers, facilitating writing into the memory cells. A read address pulse and negatively directed read select pulse are supplied to select a particular word or line to read out, activating the read decoder and lowering the potential on the word read line. This causes an increase in current flow through the cross-coupled transistors, enabling data retrieval from the memory cell. Simultaneously, a negative write select pulse is supplied to the write select line to bring the adjacent memory cell into its write-in operating state, allowing for concurrent reading and writing operations.

This innovative memory arrangement offers significant advantages in terms of rapid data transfer and simultaneous read/write access, enhancing memory access capabilities in various applications. Further research and development in this area could lead to advancements in memory system design and performance.

The work Compact dual-port dram architecture system by C. Radens et al.[15] presents an invention that introduces a process integration technology aimed at significantly reducing the array size of a dual-port DRAM architecture system. By utilizing bit lines formed at 1/2 pitch, the array size is reduced to a much smaller scale compared to conventional DRAM architecture systems. Furthermore, the invention introduces a dual-port open bit line and folded bit line DRAM array, where each DRAM cell in the array consists of at least two vertically oriented elements. In detail, the DRAM cell comprises an access transistor, a storage capacitor, a bit line, and a word line. During a write access, the access transistor is activated by a word line enable signal, allowing a data signal to be supplied to the bit line and stored in the capacitor. Conversely, during a read access, the stored data signal is routed through the access transistor to the bit line, amplified by a sense amplifier circuit, and provided to the requesting device.

One embodiment of the invention combines word lines and bit lines to prioritize and accommodate two simultaneous access requests scheduled for DRAM cells of the data array. This approach aims to suppress noise caused by overbit line coupling and bit line-substrate coupling without compromising data integrity. In cases where access requests involve read-refresh, read-read, or write operations, the system assigns higher priority to access requests scheduled through the first port than those scheduled through the second port. If two access requests involve write-read operations, equal priority is given to both requests. Consequently, the system simultaneously performs write and read accesses by accessing the corresponding DRAM cell through the first port before writing data, while simultaneously writing data through the same output bus as the read access.

This innovative approach to DRAM architecture not only reduces array size but also enhances data access efficiency and noise suppression, making it suitable for various applications requiring high-performance memory systems. Further research and development in this area could lead to advancements in memory integration technology and improved system-level performance.

IV. SUMMARY TABLE

Table 1. Summary table of review on special memory architectures.

Author(s)	Year	Memory Architecture	Key Features	Advantages	Limitations	Applications
Zhou et al. [1]	2021	Hybrid Cache with GC-eDRAM	Concurrent read/write, SRAM and eDRAM cells	Reduced energy, smaller silicon footprint	Complexity of integration	Embedded CPUs
Yiming Chen et al. [2]	2022	Fully-Concurrent Access SRAM	High row-wise parallelism, dynamic shift operations	5.5x energy efficiency, 27.2x speed increase	Design complexity, fabrication	Database updates, graph computing
Srinivasa et al. [6]	2017	3-D SRAM with Concurrent	Monolithic 3D integration,	Power and access time savings	Integration complexity	High-performance computing

		Access	multi-dimensional access			
Hiroshi Kadota and Toyonaka [9]	2014	IGFET Memory Cell	Independent read/write operations	Minimized erratic operations	Design complexity	High-speed applications
Honda et al. [10]	2014	Multi-Core Memory Cell Array	Simultaneous read/write operations, core banks	Enhanced efficiency and speed	Managing core divisions	High-speed memory access
Microsemi Corporation [11]	2011	Dual-Port SRAM for cSoCs and FPGAs	Independent operations with separate clocks	Avoids data collisions, simultaneous operations	Timing coordination complexity	Customizable SoCs, FPGAs
Subramani Kengeri and Jawji Chen [14]	2001	Pseudo Dual-Port DRAM	Simultaneous read/write in 1-T DRAM	High performance, compact size	RSA design complexity	Memory-intensive applications
C. Radens et al. [15]	2000	Compact Dual-Port DRAM	Dual-port open bit line, reduced array size	Enhanced access efficiency, noise suppression	Priority management of requests	High-performance memory systems
J. E. Gersbach [16]	1983	Simultaneous Write and Read Addressed Memory Cells	Orthogonal arrangement of decoders, direct data transfer	Rapid data transfer, simultaneous operations	Managing switching means	High-performance computing
W. R. Dachtera [17]	1978	Self-Quenching Memory Cell	Cross-coupled bipolar transistor inverters	Efficient space utilization, rapid switching	Circuit parameter adjustments	High-speed memory cells

V. CONCLUSION

Advanced Process Technologies

One promising avenue for the future development of special memory architectures is the exploration of advanced semiconductor manufacturing processes. By integrating hybrid concurrent RAM into these cutting-edge processes, significant improvements in performance and efficiency can be achieved. As semiconductor technology continues to evolve, shrinking feature sizes allow for more transistors to be packed into a smaller area, thereby enhancing the memory density and overall performance. Additionally, the use of new materials, such as high-k dielectrics and low-resistance interconnects, can further improve power efficiency and operational speed. Researchers and engineers should focus on optimizing the design and manufacturing techniques to fully exploit these advancements, potentially leading to more compact, faster, and energy-efficient memory solutions.

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Non-Volatile Integration

Another promising direction for the evolution of hybrid concurrent RAM is the integration of non-volatile memory elements. Technologies such as Magnetoresistive Random-Access Memory (MRAM) or Ferroelectric RAM (FeRAM) offer the advantage of retaining data without power, which can be incredibly beneficial for various applications. By incorporating non-volatile elements within hybrid concurrent RAM, it is possible to achieve a memory system that combines the high-speed access of traditional volatile memory with the persistence of non-volatile storage. This hybrid approach could reduce data loss risks during power outages and improve the overall reliability of memory systems. Further research is needed to address the technical challenges of integrating these non-volatile components while maintaining high-speed performance and ensuring seamless operation.

Low-Power Modes

In the quest for more energy-efficient computing systems, the development of low-power modes for special memory architectures represents a crucial area of focus. During idle periods, memory systems often consume significant power despite not being actively used. By designing low-power modes that allow the memory to reduce its power consumption during these times, overall energy efficiency can be greatly improved. These modes should be designed to ensure quick responsiveness, allowing the memory to swiftly transition back to full-power operation when needed. Techniques such as dynamic voltage and frequency scaling (DVFS), power gating, and clock gating can be employed to achieve these low-power states. Future research should aim to optimize these techniques to minimize power usage without compromising the performance and responsiveness of the memory system.

By exploring these future directions, the development of special memory architectures can continue to advance, addressing current limitations and paving the way for more efficient, reliable, and high-performance memory solutions.

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