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A HIGH EFFICIENCY MULTI-LEVEL INVERTER WITH PHASE-LOCKED LOOP TECHNIQUES

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ABSTRACT

Nowadays, use of multilevel inverters in high power applications clearly can be seen. High quality and lower distortion of the output voltage and low blocking voltage of semiconductor switches are being presented as the major privileges of the multilevel inverter compared to the traditional voltage source inverter. In our project, a new topology of multilevel inverter is proposed as fundamental block. The proposed topology is generalized using series connection of the fundamental blocks. The proposed multilevel inverter has been analyzed in both symmetric and asymmetric operation modes. A great perfection in voltage levels number with minimum switching devices has been obtained in both symmetric and asymmetric modes. Finally a computer simulation using Matlab/Simulink is presented and verifies the results.

Keywords: S H-Bridge Inverter, Cascaded H-Bridge (CHB) MLI ,Neutral Point Clamped (NPC) MLI ,Flying ,Capacitor MLI ,Gate Driver Circuit ,MOSFET / IGBT Switching ,Voltage Balancing ,Phase Disposition PWM (PD-PWM) ,Phase Opposition Disposition PWM (POD-PWM) ,Level-Shifted PWM (LS-PWM) ,Space Vector Modulation (SVM).

I. INTRODUCTION

Multilevel inverters (MLIs) have gained significant attention in high-power and medium-voltage applications due to their superior performance compared to traditional two-level voltage source inverters (VSIs). These inverters generate stepped output voltage levels, which help in reducing harmonic distortion, improving power quality, and minimizing voltage stress on power semiconductor devices. MLIs are widely used in renewable energy systems, electric vehicles, industrial motor drives, and grid-connected applications due to their ability to handle high voltage and power efficiently.

There are several types of multilevel inverter topologies, including **Diode-Clamped Multilevel Inverter (DCMLI), Flying Capacitor Multilevel Inverter (FCMLI), and Cascaded H-Bridge Multilevel Inverter (CHBMLI)**. Each topology has its advantages and limitations. The diode-clamped inverter uses multiple clamping diodes to stabilize voltage levels, while the flying capacitor inverter utilizes capacitors for voltage balancing. The cascaded H-bridge inverter, on the other hand, consists of multiple H-bridge cells connected in series to achieve higher voltage levels with reduced harmonic distortion.

Despite their advantages, traditional multilevel inverters have certain drawbacks, such as an increased number of power components, complex control strategies, and high cost due to additional semiconductor switches, capacitors, and diodes. Moreover, balancing the capacitor voltage and ensuring proper switching sequences can be challenging, particularly in high-level configurations.

To address these challenges, our project proposes a novel multilevel inverter topology that minimizes the number of switching devices while enhancing output voltage quality. The proposed topology is analyzed in both symmetric and asymmetric modes, achieving a greater number of voltage levels with fewer components. A MATLAB/Simulink-based simulation is conducted to verify the effectiveness of the proposed inverter, demonstrating its superior performance in terms of reduced switching losses, improved efficiency, and enhanced harmonic /performance.

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II. PROPOSED SYSTEM

Fig. 1 shows the fundamental block of proposed topology. As can be seen in Fig. 1 the basic block of proposed multilevel inverter consists of 2 dc voltage sources. Generally, the voltage sources can be unequal. If dc voltage sources have same voltages, the basic block will be analyzed in symmetric mode. In this case, the dc voltage sources are considered to be equal to dc V . The asymmetric analyzes are carried out when the dc sources have different values. The basic block includes 6 semiconductor switches. Each switch should be connected to an anti-parallel diode. As a practical solution, insulated gate bipolar transistor (IGBT) with an anti-parallel diode can be used instead of each switch and relative diode. In addition to mentioned ingredients and to have proper operation of circuit, 8 diodes should be employed. As a matter of fact, anti-parallel diodes and 8 independent diodes are undertaken conduction of backward current. Backward current is caused by inductive characteristic of load

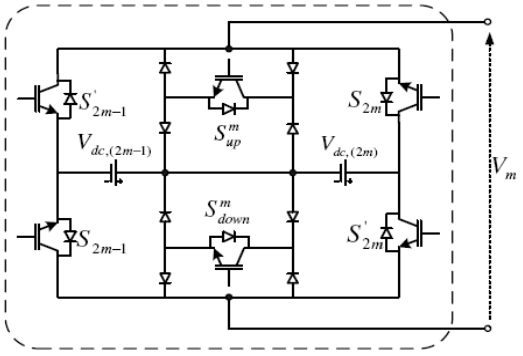

Fig. 1. Fundamental block of proposed multilevel inverter

Fig. 1 shows, The IGBTs are named purposely in Fig. 1. It is considered the depicted block is the M th block of a generalized multilevel inverter. Hence, if the block is supposed as first block, the names are replaced with

$$\mathbf{S_1, S_1^`, S_2, S_2^`, S_{up}^1, S_{down}^1, V_{dc,1}, V_{dc,2}, V_1}$$

The fundamental block can be operated in either symmetric or asymmetric modes.

A) Symmetric Mode

Table 1 Output Voltage and Switches State For Symmetric Mod

State number	Switches state						Output voltage
	S_{2m-1}	S'_{2m-1}	S_{2m}	S'_{2m}	S^m_{up}	S^m_{down}	
1	1	0	1	0	0	0	$+2V_{dc}$
2	1	0	0	0	1	0	$+V_{dc}$
	0	0	1	0	0	1	
3	0	0	0	1	0	0	0
	0	0	1	0	0	0	
	1	1	0	0	0	1	
4	0	1	0	0	0	1	$-V_{dc}$
	0	0	0	1	1	0	
5	0	1	0	1	0	0	$-2V_{dc}$

In symmetric mode, all dc voltage sources are equal to dc V . The basic block can generate 5 levels in output voltage. Turning the appropriate switches on or off produces the expected level on the output voltage. It is notable that, aforementioned 5 levels are zero, 2 positive and 2 negative voltage levels. Switching pattern for symmetric operation of basic block is illustrated in Table 1.

As it can be seen in Table 1 there are redundant switching states for 3 of voltage levels. These redundancies in switching states can provide possibilities for average power controlling in proposed

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multilevel inverter in symmetric mode.

B) Asymmetric Mode

If the values of dc voltage sources are chosen to be different, the presented basic block is to be operated in asymmetric mode. The asymmetric mode analyzes are carried out by applying following equation to determine amount of voltage sources:

$$V_{dc,(2m)} = 2V_{dc,(2m-1)}$$

In this case, 7 voltage levels are obtained on the output of basic block. As it was demonstrated in symmetric mode, the zero, 3 positive and 3 negative levels are generated on the output voltage of basic block in the asymmetric mode.

Table 2 shows different states of switches and the produced voltage on fundamental block output.

Output Voltage And Switches States for Asymmetric Mode (Table 2)

State number	Switches state						Output voltage
	S_{2m-1}	S'_{2m-1}	S_{2m}	S'_{2m}	S^m_{up}	S^m_{down}	
1	1	0	1	0	0	0	$+3V_{dc}$
2	0	0	1	0	0	1	$+2V_{dc}$
3	1	0	0	0	1	0	$+V_{dc}$
4	0	0	0	0	1	1	0
5	0	1	0	0	0	1	$-V_{dc}$
6	0	0	0	1	1	0	$-2V_{dc}$
7	0	1	0	1	0	0	$-3V_{dc}$

The generalized proposed multilevel inverter is constructed by series connection of several fundamental blocks. Series connection of blocks increases the number levels. Fig. 2 depicts generalized proposed multilevel inverter. Two modes of exploitation are possible for proposed multilevel inverter: The symmetric and asymmetric mode.

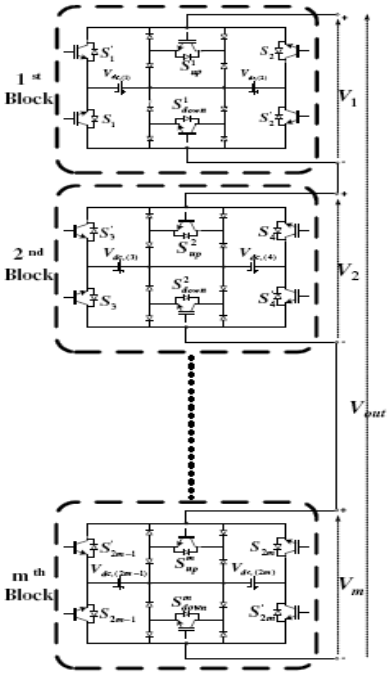

Fig. 2. Topology of proposed multilevel inverter

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A) Symmetric Operation

Symmetric multilevel inverter is considered to be made by series connection of n symmetric basic blocks. The overall output voltage is equal to summation of output voltages of n blocks. The following equations can be written in symmetric mode

$$V_{dc,(k)} = V_{dc} \quad (2)$$

$$V_{max}^{m} = 2V_{dc} \quad (3)$$

$$V_{max}^{m} = 2nV_{dc} \quad (4)$$

Where, V_{max}^{m} is t he maximum voltage on the output of m^{th} block and V_{max} is the maximum produced voltage by proposed symmetric multilevel inverter. It can be derived, the overall output voltage varies from

$$-V_{max} \text{ to } +V_{max}$$

In this mode number of levels is obtained as follow:

$$N_{level} = 4n+1$$

$$N_{source} = 2n$$

All possible states for a symmetric multilevel inverter are shown in Table 3.

(Table 3) Possible states for symmetric proposed multilevel inverter

State Number	Output voltage of blocks					Output Voltage
	1	2	…	$m-1$	m	
1	$+V_{dc}$	$+V_{dc}$	…	$+V_{dc}$	$+V_{dc}$	$+2nV_{dc}$
2	$+V_{dc}$	$+V_{dc}$	…	$+V_{dc}$	0	$+(2n-1)V_{dc}$
⋮	⋮	⋮	⋮	⋮	⋮	⋮
$2n+1$	0	0	…	0	0	0
⋮	⋮	⋮	⋮	⋮	⋮	⋮
$4n$	0	$-V_{dc}$	…	$-V_{dc}$	$-V_{dc}$	$-(2n-1)V_{dc}$
$4n+1$	$-V_{dc}$	$-V_{dc}$	…	$-V_{dc}$	$-V_{dc}$	$-2nV_{dc}$

In account of organized and cascaded structure of proposed topology, all modulation methods that are applicable in multilevel inverters are applicable in proposed multilevel inverter in symmetric mode, too. According to aforementioned equations, for a proposed symmetric multilevel inverter which is consisted of 2 basic blocks the following calculations can be written:

$$V_{max} = 4V_{dc}$$

$$N_{level} = 9$$

It is obvious, in this example $4\ dc$ sources are required and number of switches is 12. Fig. 3 shows the simulation results for mentioned example. V_{dc} is supposed to be 100V.

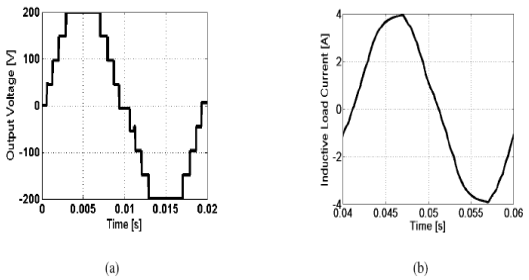

Fig. 3. Simulation Result of 9-Level Proposed Symmetric Multilevel Inverter

(a) Output Voltage (b) Load Current

B) Asymmetric Operation

Series connection of n asymmetric blocks or n symmetric blocks with different dc voltage sources builds an asymmetric proposed multilevel inverter. As mentioned before, dc voltage sources have different value in asymmetric mode. As a matter of fact, the difference between values of sources improves performance of

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multilevel inverter and enhances the number of levels. In practical applications, distinct dc voltage sources can be available in different ways.

For instance, employing PV arrays or using a transformer with multiple isolated outputs or applying fuel cells can be considered. Series and parallel connection of PV cells or using DC/DC converters on their outputs brings about distinct values of voltage. To exploit PV arrays effectively and to get the maximum energy in different conditions and also to provide demanded current in DC side of proposed inverter, use of battery banks seems to be necessary. In addition, different turn ratios for secondary windings of transformer provide different values of dc voltage sources. In this case the important subject is to choose value of dc voltage sources. There are lots of choices for values of dc voltage sources. The asymmetric mode can be analyzed in three cases. The hardware structures are the same in all cases. The difference is just in the value of dc voltage sources.

Losses Study

IGBT and diode losses, as well as power losses in any other semiconductor component, can be divided in three groups:

1. Conduction losses (P_{cond})
2. Switching losses (P_{sw})
3. Blocking losses (P_b)

Conduction losses are caused by equivalent resistance and the on-state voltage drop of the semiconductor device. The switching losses are related to non-ideal operation of switches. Blocking losses which is caused by leakage current in off-state of IGBT, can be normally neglected. Therefore total power losses can be calculated as follow]:

$$\mathbf{P_{loss}} = \mathbf{P_{cond}} + \mathbf{P_{sw}}$$

Power losses calculations for the proposed multilevel inverter in symmetric and asymmetric forms are the same. It is obvious that, not only power loss in a power

converter depends on power semiconductors characteristics but also it depends on switching algorithm. As prerequisites of losses calculations, it is assumed that the multilevel inverter is controlled by pulse width modulation (PWM) control based on comparison of sine-wave and saw-tooth wave and also the output current of inverter is ideal sin-wave form.

1. Conduction losses

As the first step of calculations, the conduction power losses of a typical power semiconductor switch and diode are carried out and thereafter they are developed to the proposed multilevel inverter.

$$I_c = \sqrt{2} I_M \sin(\omega t)$$

$$V_{CE} = V_T + R_T I_C$$

$$V_{FWD,AK} = V_{FWD} + R_D I_{FWD}$$

$$P_{c.T} = \frac{D_T}{\pi} \int_0^{\pi} I_C V_{CE} d\theta = \frac{1}{2} D_T \left[\frac{2\sqrt{2}}{\pi} I_M V_T + I_M^2 R_T\right]$$

$$P_{c,FWD} = \frac{1}{2} D_{FWD} \left[\frac{2\sqrt{2}}{\pi} I_M V_{FWD} + I_M^2 R_{FWD}\right]$$

$$P_{c,Ind-D} = \frac{1}{2} D_{Ind-D} \left[\frac{2\sqrt{2}}{\pi} I_M V_D + I_M^2 R_D\right]$$

where DT , DFWD and DInd - D are average conductivities of the IGBT, free wheel diode and independent diode at a half cycle of output current. Additionally, V CE and V FWD AK , are the ON-state voltages of IGBT and free wheel diode respectively. R T , R FWD and R D are the equivalent resistances of the IGBT, free wheel diode and independent diode and V T FWD ,V and V D represent IGBT on-state zero-current collector-emitter voltage, free wheel diode zero-current voltage and independent diode zero current voltage, respectively.

In proposed multilevel inverter number of ON-state IGBTs and forward biased diodes are depend on voltage level and current direction so it is variable by time. Considering the current commutation in a basic block and depending the output voltage level there might be 2 IGBTs or 2 IGBTs and 2 diodes in current path. Fig. 9 shows the current path for 2 voltage level in a basic block. To producing the maximum voltage levels

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$(-V_{max}, +V_{max})$ in a basic block, just 2 IGBTs are being serially connected but 2 diodes are added to the current path for generating other voltage levels. The average conduction power loss of the proposed multilevel inverter can be calculated with applying equation (28), (29), (30) as follows:

$$P_c = \sum_{j=1}^{N_D}\sum_{i=1}^{N_{sw}}\left[\frac{\sqrt{2}}{\pi} I_M V_O\left(D_{T,i} + D_{FWD,i} + D_{D,j}\right) + \frac{1}{2} I_M^2 \left(D_T, i^R T, i + D_{FWD,i} R_{FWD,i} + D_{Ind-D,j}{}^R{}_{Dj}\right)\right]$$

Where, N D and N sw are the total number of independent diodes and IGBTs respectively. Parameters i refer to i th switch or free wheel diode and j refer to j th independent diode. It is noted that to simplify the calculation, the V T ,V FWD and V D are supposed to be the same and equal to V O in (31).

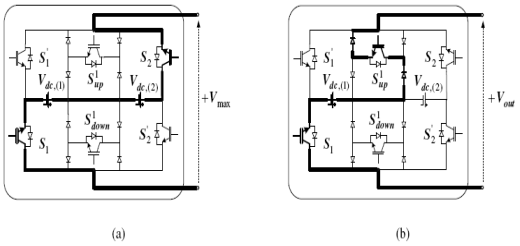

Fig. 9. (a) Current path for generating +V max (b) Current path for generating Vout

2. Switching losses

As carried out in previous calculation, the switching power losses of the proposed multilevel inverter are calculated by extending the switching losses of typical IGBT. To calculate the switching losses the linear approximation of voltage and current during turn-on and turn-off period is used. Therefore energy loss during the turn-on and turn-off period of a switch can be formulated as follows [23]:

$$\mathbf{E_{on,T}} = \int_0^{t_{on}} \mathbf{v(t)i(t)dt} = \int_0^{t_{on}} \left[\left(\frac{\mathbf{V_{sw,T}}}{\mathbf{t_{on}}}\mathbf{t}\right)\left(-\frac{\mathbf{I}}{\mathbf{t_{on}}}(\mathbf{t}-\mathbf{t_{on}})\right)\right]\mathbf{dt} = \frac{\mathbf{1}}{\mathbf{6}}\mathbf{V_{sw,T}I\,t_{on}}$$

$$\mathbf{E_{off,T}} = \int_0^{t_{off}} \mathbf{v(t)i(t)dt} = \int_0^{t_{off}} \left[\left(\frac{V_{sw,T}}{t_{off}}t\right)\left(-\frac{I}{t_{off}}(t-t_{off})\right)\right]dt = \frac{1}{6}V_{sw,T}I\,t_{off}$$

Generally, total switching power losses of a fundamental block can be calculated as below:

$$P_{sw} = 2f\left[\sum_{k=1}^{N_{sw}}\left(\sum_{i=1}^{N_{on,k}} E_{on,k,i} + \sum_{i=1}^{N_{off,k}} E_{off,k,i}\right)\right]$$

where f is the fundamental frequency, N on k , and N off k ,are the number of turning on ON and OFF the switch k during a half fundamental cycle. Also E on k i, , is the energy loss of the switch k during the i th turning ON and E off k i, is the energy loss of the switch k during the th i turning OFF.

III. MATERIALS AND METHODS

1. Materials Used

1.1 Electronic Components

Microcontroller – PIC, Arduino, or DSPIC (for generating PWM signals).

MOSFETs / IGBTs – Power switching devices (e.g., IRF540, IRF3205, or IGBT modules).

Gate Driver ICs – IR2110, TLP250, or optocoupler-based drivers for safe switching.

Capacitors – Filtering com

Resistors – Used for voltage division and current limiting.

Diodes – For rectification and freewheeling (e.g., 1N4007, FR107).

Transformers – Step-down transformers for AC voltage conversion.

Voltage Regulators – 7805, 7812 (for stable power supply).

Heat Sinks – For cooling MOSFETs/IGBTs and preventing overheating.

1.2 Power Supply & Measurement Equipment

DC Power Supply – Multi-level voltage sources (e.g., 12V, 24V, 48V).

Oscilloscope – To analyze output waveform and frequency response.

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Multimeter – To measure voltage, current, and resistance.

Load (Bulbs or Resistors) – To test inverter performance under load conditions.

1.3 Software & Simulation Tools

Proteus / MATLAB Simulink – For circuit simulation and waveform analysis.

Arduino IDE / MPLAB / Keil – For microcontroller programming.

2. Methods

2.1 Circuit Design & Simulation

1. Design the H-Bridge Topology:

The inverter is based on a Cascaded H-Bridge (CHB) configuration to generate multiple voltage levels.

The switching logic is controlled by a microcontroller using Pulse Width Modulation (PWM).

2. Simulation in Proteus / MATLAB:

The circuit is simulated to verify the stepped waveform before hardware implementation.

The Total Harmonic Distortion (THD) is analyzed to ensure power quality

2.2 Hardware Implementation

1. Microcontroller Programming:

A microcontroller (PIC/Arduino/DSPIC) is programmed to generate switching pulses.

PWM techniques like Phase Disposition PWM (PD-PWM) or Sinusoidal PWM (SPWM) are implemented.

2. Gate Driver Circuit Setup:

Gate driver ICs (IR2110 or TLP250) are used to provide proper voltage levels to MOSFETs/IGBTs.

Optocouplers ensure isolation between control and power circuits.

3. H-Bridge Power Circuit Assembly:

Multiple H-bridge modules are connected in series to form the 15-level inverter.

MOSFETs/IGBTs are heat sink mounted to prevent thermal issues.

4. Transformer & Load Connection:

The AC output is fed to a step-up transformer to match desired voltage levels.

The output is tested under different load conditions (resistive & inductive).

2.3 Testing & Output Waveform Analysis

1. Oscilloscope Measurement:

The output waveform is measured using an oscilloscope.

The frequency (~50-60Hz) and voltage levels (stepped waveform) are verified.

2. THD & Power Quality Analysis:

The quality of the AC output waveform is analyzed.

The harmonic content is measured using FFT analysis in MATLAB.

3. Performance Under Load:

The inverter is tested with resistive (bulb) and inductive (motor) loads to evaluate efficiency.

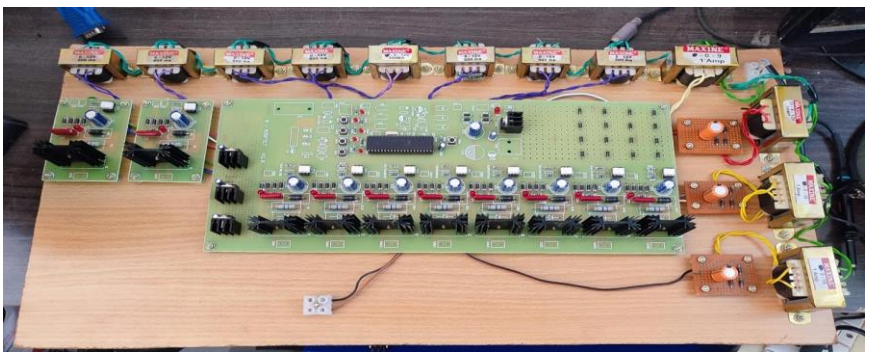

Fig 1: Project Kit

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IV. RESULTS AND DISCUSSION

The Proposed multilevel inverters are designed and simulated on MATLAB Simulink platform. The following section deeply explains the basic fundamentals of MATLAB Simulink toolbox and consequence sections clearly describing the` Simulink model representations and the obtained output waveforms of aforementioned inverter models.

The following figure represents the overall topology of the 15 level inverter.

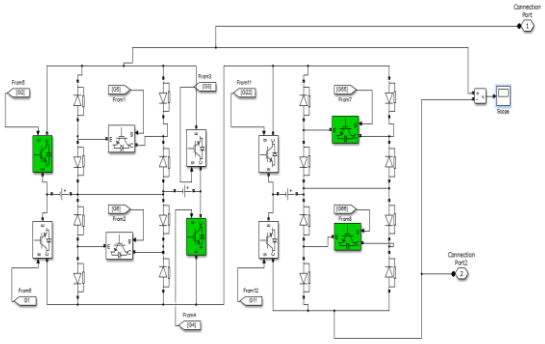

Figure 4.1 Simulink model for symmetrical 15 level inverter

The switches of the proposed topology are switched by the sinusoidal PWM technique and the switching pattern generation block is shown in below figure. As mentioned in previous section, the symmetrical configuration can be declared with the similar voltage levels as a DC input. The following figure depicts the DC input voltage values on MATLAB Simulink.

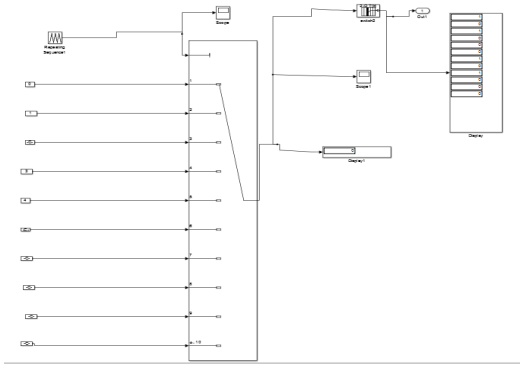

Figure 4.2 switching block model for 15 level inverter

The obtained output AC voltage is shown following figure and it clearly explains that a single waveform is having 15 levels.

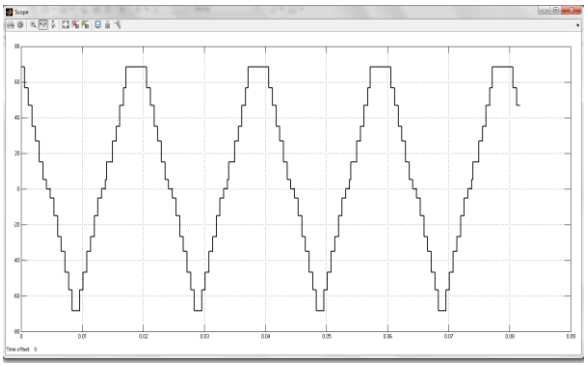

Figure 4.3 output voltage for 15 level inverter

V. CONCLUSION

A new multilevel inverter topology has been proposed in this project. The proposed topology has superior features over conventional and recently published new topologies in terms of the required power

semiconductor switches, isolated dc supplies, number of output voltage level, driver number, total power losses and cost. Because of substantial increase in voltage levels with less semiconductor switches this topology can be a good candidate for converters used in power applications especially in high voltage applications. In the mentioned topology, the switching operation is separated into high and low frequency parts. The implemented multilevel circuit has been tested in different operation modes. Hence the simulation and experimental results of the developed prototype for 15-level, operation modes are simulated in the project.

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