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INTEGER-N RF SYNTHESIZER AND FREQUENCY DIVIDER

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ABSTRACT

In an RF communication system, the oscillators are the essential component to provide synchronization between transmitter and receiver. Oscillators used in RF transceivers are usually embedded in a 'synthesizer' environment to precisely define their output frequency. Synthesizer design has for decades proved a difficult task, leading to hundreds of RF synthesis techniques. The PLL (Phase Locked Loop) based synthesizers generally provide better stability with closed-loop control. The PLL concept improves the performance of the synthesizer circuit with additional spur reduction techniques. The use of 'Frequency Divider' in a feedback loop provides frequency selectivity to a synthesizer. In the RF IC domain, the synthesizers are classified into two major categories namely 'Integer-N' synthesizers and 'Fractional-N' synthesizers. This article provides designing of an integer-N Synthesizer using a frequency divider in LTspice software.

Keywords: RF Synthesizer, Frequency Divider, RF IC, PLL, VCO.

I. INTRODUCTION

A frequency synthesizer allows the designer to generate a variety of output frequencies as multiples of a single reference frequency. The main application is in generating local oscillator (LO) signals for the up-and down-conversion of RF signals. Frequency synthesizers are used in a host of different RF equipment - almost anywhere that a stable RF source is required. RF frequency synthesizers provide high levels of performance in terms of stability, programmability and general convenience and performance. As a result, the different types of frequency synthesizers are used increasingly in all forms of RF circuit design. As most equipment requiring the use of an RF synthesizer also has digital circuitry for other elements of the device, RF synthesizers lend themselves particularly well to being used - various types have digital circuitry in them and interfacing them to processors and other digital circuitry for ease of control and flexibility.

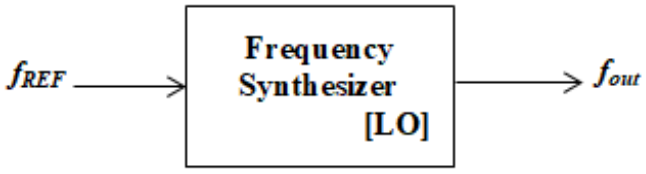

Fig 1.1 : Generic frequency synthesizer

Figure 1.1 shows the conceptual picture of a generic frequency synthesizer. The output frequency is generated as a multiple of a precise reference, fREF, and this multiple is changed by the channel selection command to cover the carrier frequencies required by the standard. In addition to accuracy and channel spacing, several other aspects of synthesizers impact a transceiver's performance: phase noise, sidebands, and lock time [1]. The PLL based frequency synthesizers are well suited for a generation of a required frequency and its integer multiples considering all the designing aspects. The PLL controls the settling time and provides some additional spur reduction techniques to control the VCO (Voltage Controlled Oscillator) free-running frequency. The frequency divider block in the feedback path of a PLL allows a channel selection strategy to obtain the desired frequency for the synchronization between the sender and receiver sides. The designing of a frequency divider is an important aspect as it is responsible for a multiple frequency generation from a locked PLL frequency. The Integer-N frequency synthesizers and fractional-N frequency synthesizers or the combination of two are the essential building blocks of a local oscillator circuit in the RF domain. In Frequency hopping CDMA, SDR (Software Defined Radio), and small cell–micro base stations, the frequency synthesizer circuit provides greater stability, higher speed of operation and accuracy in the channel selection to enhance RF communication. RF synthesizers with frequency divider concept provide advancement in network analyzers and spectrum analyzers for a better operation.

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II. METHODOLOGY

Integer-N synthesizers produce an output frequency that is an integer multiple of the reference frequency. If N increases by 1, then fout increases by fREF; i.e., the minimum channel spacing is equal to the reference frequency. Figure 2.1 shows the block diagram of an integer-N frequency synthesizer with frequency divider.

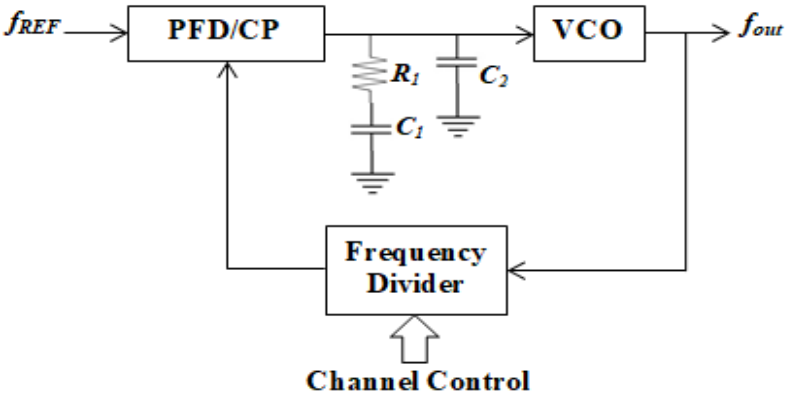

Fig 2.1 : Block diagram of an integer-N frequency synthesizer

PFD/CP:

Phase frequency detector is one of the important parts in PLL circuits. PFD (Phase Frequency Detector) is a circuit that measures the phase and frequency difference between two signals i.e., the signal that comes from the VCO and the reference signal. PFD has two outputs UP and DOWN which are signaled according to the phase and frequency difference of the input signals. The output signals of the PFD are fed to the CP (Charge Pump). The output voltage of the charge pump controls the output frequency of the VCO, so with a change happens at the input of the CP the output voltage will change which will change the output frequency of the VCO [4].

Filter Section:

A Low Pass Filter (LPF) is used in PLL to get rid of the high frequency components in the output of the phase detector. It also removes the high frequency noise. All these features make the LPF a critical part in PLL and helps control the dynamic characteristics of the whole circuit. The dynamic characteristics include capture and lock ranges, bandwidth, and transient response. The lock range is the tracking range where the range of frequencies of the PLL system follows the changes in the input frequency.

VCO:

The voltage-controlled oscillator performance governs many aspects of the performance of the whole phase locked loop or frequency synthesizer. The VCO generates the output signal. It is maintained at the setpoint frequency by the PLL and locked to the reference frequency. The range of input frequencies over which PLL will capture the input signal is referred as PLL capture range. Both PLL lock range and PLL capture range are centered around the VCO free running frequency [5].

Frequency Divider:

PLL based frequency synthesizers make use of frequency dividers to generate a frequency that is a multiple of a reference frequency. A common realization of the feedback divider that allows unity steps in the modulus is called the pulse swallow divider. A dual-modulus pre-scaler counter provides a divide ratio of (N + 1) or N according to the logical state of its modulus control input. A swallow counter circuit divides its input frequency by a factor of S, which can be set to a value of 1 or higher in unity steps by means of the digital input. This counter controls the modulus of the pre-scaler and also has a reset input. A program counter divider has a constant modulus, P. When the program counter fills up (after it counts P pulses at its input), it resets the swallow counter [1]. Figure 2.2 shows the frequency divider realization using pulse swallow divider.

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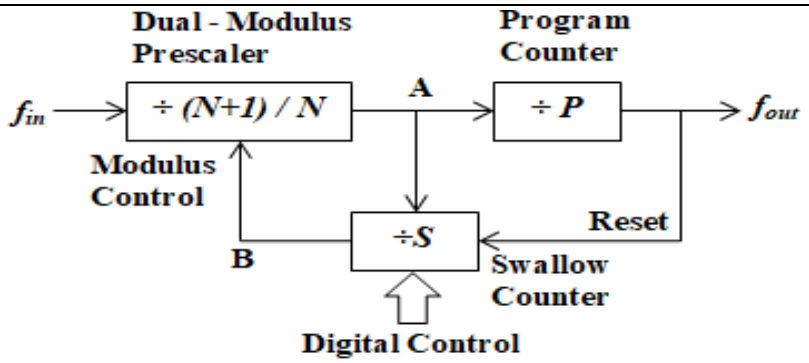

Fig 2.2 : Pulse swallow divider

In modular divider realization, the divider employs 'n ÷ 2/3' blocks, each receiving a modulus control from the next stage (except for the last stage). Figure 2.3 represents the actual realization of a modular divider with multiple divide ratios.

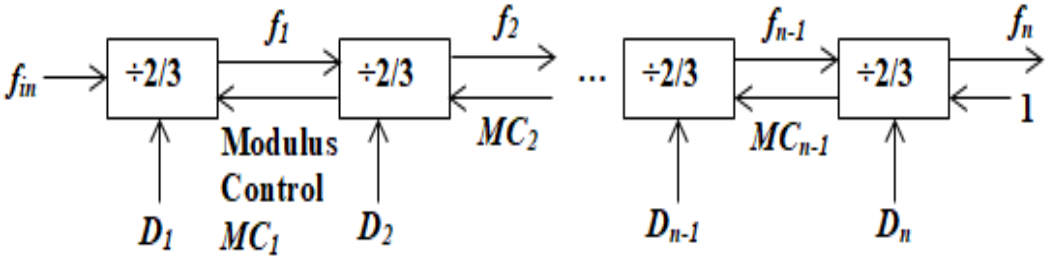

Fig 2.3 : Modular divider realization using multiple divide ratios

The digital inputs set the overall divide ratio according to $N = 2^n + D_n 2^{n-1} + D_{n-1} 2^{n-2} + \ldots\ldots + 2D_2 + D_1$

III. MODELING AND ANALYSIS

The modeling and designing of a frequency divider are done by considering a fact that the flip-flop acts as a divide by 2 circuit.

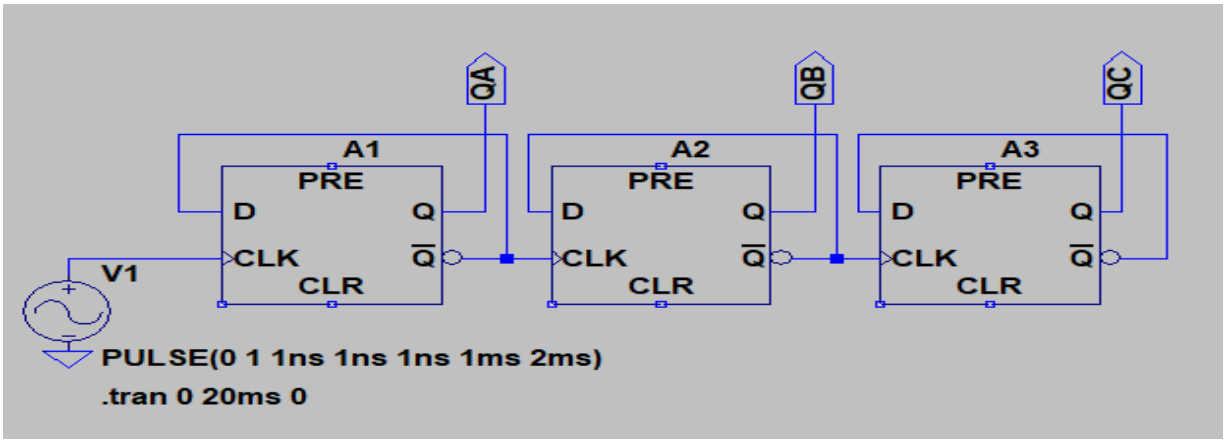

Fig 3.1 : Design model for a frequency divider in LTspice

The signal applied as a CLK input to the first flip-flop acts a fundamental frequency. At the output of each flip-flop the fundamental frequency gets divide by the factor of N. The frequency divider circuit represents divide by N block in the synthesizer block diagram. The output stage of first flip flop (QA) provides the frequency which is an integer multiple of 2 of the original frequency. Similarly, the QB and QC stages represents the divide by N ratio frequencies according to the flip-flop stage sequence number. Figure 3.1represents LTspice model for frequency divider realization.

The integer-N frequency synthesizer is designed using PLL with the frequency divider block in a feedback path. In the modeling of a synthesizer, the first block PFD is represented by a current-dependent current source with

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the value of 50 uA. The filter section is designed with two capacitors and a resistor. (C1: 22 nF, C2: 470 pF, R1: 10 (ohm)). The VCO is represented by a voltage-dependent voltage source with specifications E1: Laplace = 20meg/s [2]. Figure 3.2 shows the PLL based integer-N synthesizer model in LTspice.

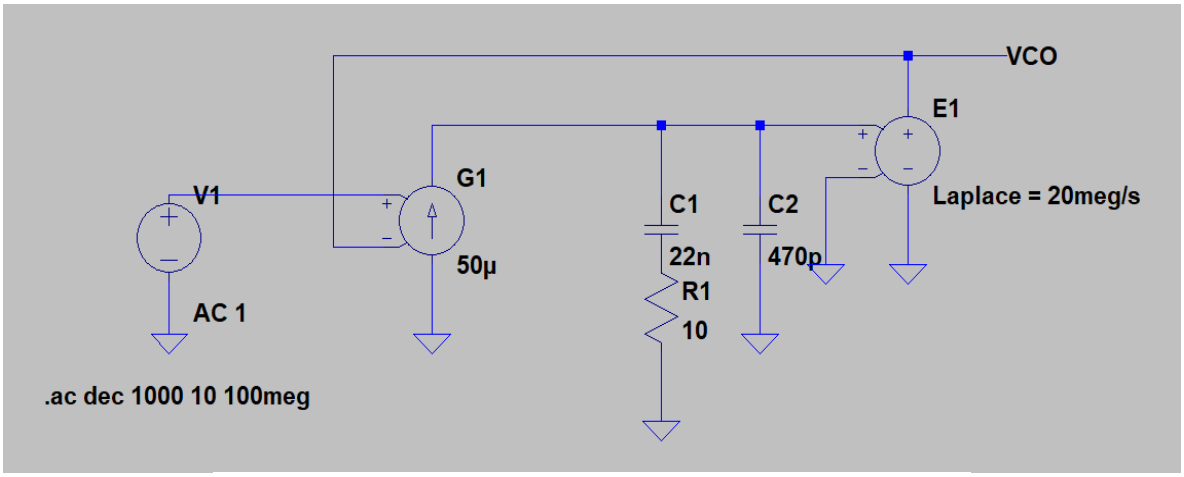

Fig 3.2 : LTspice circuit model for an integer-N frequency synthesizer

The desired frequency is obtained at the VCO output after the VCO settling time is completed. For better stability, the VCO frequency should be the same as that of the frequency divider output frequency. In the RF domain, the suitable channel is selected by achieving frequency synchronization with the help of synthesizer output.

IV. RESULTS AND DISCUSSION

The frequency divider circuit is realized using an arrangement of the flip-flops in a cascading manner. Each output stage of flip-flop divides the input clock frequency by the factor of multiple of 2. Figure 4.1 shows the frequency division of the CLK frequency for each output stage of cascading arrangement.

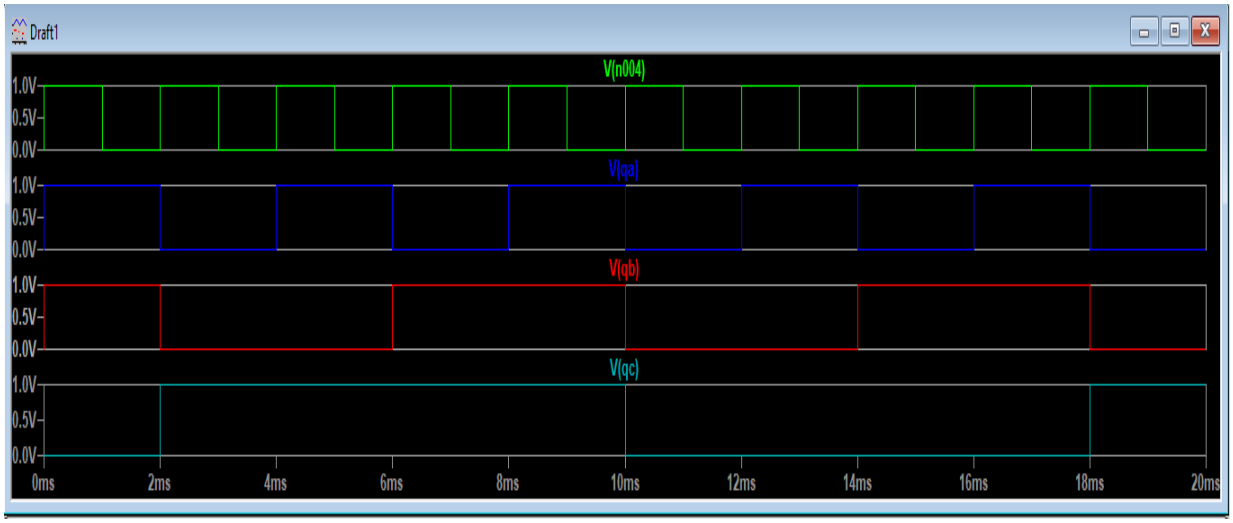

Fig 4.1 : Frequency divider output

The desired value of 'N' can be selected and the respective frequency can be fed into the feedback path of a PLL to construct an RF synthesizer. For excellent synchronization between the transceivers, the LO (Local Oscillators) should generate a stable frequency using a synthesizer. The stability of a synthesizer can be tested by plotting frequency response characteristics using the 'Bode-plot' technique. Figure 4.2 shows the bode plot of an integer-N synthesizer circuit for frequency ranges in the RF domain.

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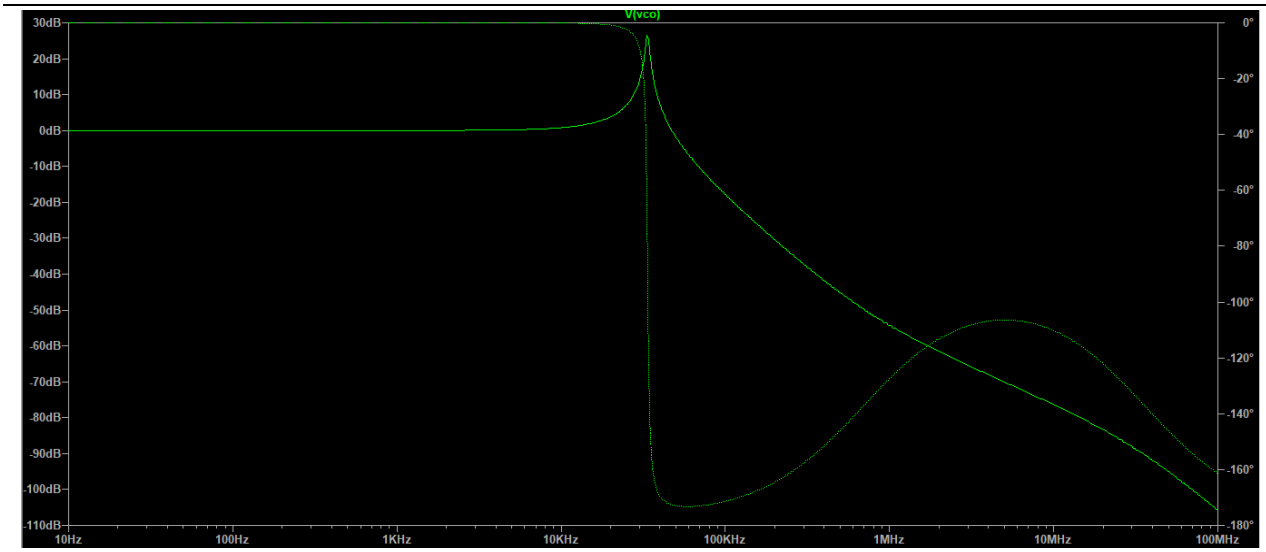

Fig 4.2 : Integer-N RF synthesizer output

Particular frequency is obtained from the RF range and the stability is tested by the bode-plot technique. Further, the stability check is possible by calculating GM (Gain Margin) and PM (Phase Margin) from the frequency response analysis.

V. CONCLUSION

The PLL based RF synthesizers using frequency dividers are best suited to generate synchronized carriers from the LO building block in the RF communication system. The frequency dividers can be realized using cascading of flip-flops as flip-flop acts as a divider by 2 circuits. Frequency divider circuits provide channel selectivity function to the synthesizer circuit when used in the feedback path. The integer-N RF synthesizer proposed in this article generates a stable, distortion-less, noise immune suitable frequency for the effective synchronization in transceivers in RF domain applications. Moving to programmable frequency dividers using FPGA logic will further enhance the operational speed and response of an RF Synthesizer.

VI. REFERENCES

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