

SIMULATION STUDY OF A SEVEN-LEVEL INVERTER WITH SINUSOIDAL PULSE WIDTH MODULATION

Deepak Kumar. R*¹, Hitesh Balaji. N*², Kavlin. M*³

*^{1,2,3}Student, Sri Ramakrishna Engineering College/Electrical And Electronics Engineering, Coimbatore, India.

DOI: <https://www.doi.org/10.56726/IRJMETS63835>

ABSTRACT

This paper explores the design, analysis, and simulation of a single-phase, seven-level inverter developed to improve upon traditional inverter technologies by enhancing efficiency and reducing harmonic distortion. This advanced inverter utilizes Sinusoidal Pulse Width Modulation (SPWM) in conjunction with a cascaded H-bridge configuration, enabling precise control over the output waveform. With dual operational modes—fundamental frequency and high-frequency switching—the inverter is optimized for versatility in handling various load demands, making it especially suited to high-quality power applications where efficiency and stability are critical. Traditional inverters, typically limited to two or three levels, often face challenges such as high switching losses, increased harmonic distortion, and suboptimal efficiency. To address these issues, this inverter adopts a multilevel design. By incorporating additional levels in the output waveform, the seven-level inverter significantly improves waveform quality, achieving reduced Total Harmonic Distortion (THD), which is crucial for stable and efficient power output. The cascaded H-bridge architecture facilitates this by generating multiple voltage levels that result in a smoother waveform, minimizing harmonic interference and improving overall power quality. At the core of this inverter's operation is SPWM, a widely used modulation technique known for its ability to generate high-quality AC waveforms from DC inputs. SPWM operates by adjusting the width and timing of the switching pulses, effectively controlling the inverter's switches to produce an AC output that approximates a sinusoidal waveform. This method not only reduces switching losses but also enables a high level of harmonic suppression. The SPWM control, in combination with the cascaded H-bridge structure, enhances the inverter's ability to meet strict power quality requirements, especially for applications demanding stable and clean power. The inverter's performance is rigorously tested through MATLAB simulations, which allow for the examination of various load conditions, including rapid load changes. These simulations are crucial in assessing how the inverter adapts to real-world conditions, ensuring that it maintains stable and efficient performance under fluctuating demands. The MATLAB simulation environment provides a detailed view of the inverter's response, enabling analysis of its behavior across different operational scenarios. Simulation results reveal that the inverter successfully maintains a THD as low as 10%, a notable improvement over traditional two-level inverters. This low THD contributes to a cleaner waveform, which is essential for stable power delivery and minimizes potential interference with other equipment. The simulations also show that the inverter effectively handles abrupt load changes with minimal impact on output stability. Its fast transient response and ability to quickly stabilize output after load variations highlight the robustness of the design, making it suitable for environments where load conditions fluctuate unpredictably. The consistent performance under varied loading conditions confirms that the inverter's seven-level output, achieved through SPWM and cascaded H-bridge configurations, achieves the intended reduction in THD while maintaining efficient power conversion. These simulation findings underscore the design's effectiveness and its potential as a viable solution for power systems requiring high-quality and reliable AC output. In summary, this paper presents a single-phase, seven-level inverter design that demonstrates substantial improvements in efficiency and harmonic reduction over conventional inverter models. Utilizing SPWM with a cascaded H-bridge configuration, the inverter achieves low THD and effective handling of load changes. MATLAB simulations confirm that the design maintains stable and efficient performance across varied operational conditions, highlighting its ability to meet modern power quality standards and address critical challenges in inverter technology. Future research could focus on further optimization of the design, exploring alternative modulation strategies, and potentially scaling the inverter for three-phase applications to extend its usability in a broader range of power systems.

Keywords: Single Phase H-Bridge Seven Level Inverter, Switching Frequency, Sinusoidal Pulse Width Modulation, And Total Harmonic Distortion (THD).

I. INTRODUCTION

For years, large inverters have been the backbone of powering heavy-duty industrial operations, handling the ever-growing demand for high-power applications ranging from tens to hundreds of megawatts. Consider medium-voltage AC motor drives operating in the 2.3 to 13.8 kV range. As businesses have evolved, the rising voltage levels have made it increasingly challenging to connect even a single power-based semiconductor switch directly to the grid. To address this issue, a new power converter has emerged, specifically designed for high-power applications. These innovative devices utilize lightning-fast switching components, circumventing the complexities of direct grid connections by distributing single devices across multiple DC levels. Multilevel converters are employed in a variety of applications, including utility settings for sustainable energy sources like fuel cells, wind, and solar, as well as in industrial motor drive systems. They play a crucial role in systems like FACTS, HVDC transmission, and traction drive setups. This paper provides a comprehensive explanation of the operation and hardware implementation of a seven-level inverter.

II. LITERATURE SURVEY

1. In grid-connected photovoltaic (PV) systems, Villanueva, Correa, Rodríguez, and Paces (2009) describe a control technique for a cascaded H-bridge in single phase. Effective maximum power point tracking (MPPT) for various PV module strings is made possible by this method by permitting the independent regulation of each DC-link voltage. The study highlights the benefits of the cascaded H-bridge architecture, including increased adaptability, scalability, and power quality.
2. The work by Malinowski et al. (2010) focuses on the design, control schemes, and applications of cascaded multilevel inverters. It highlights how their versatility, redundancy, and excellent output quality make them ideal for high-power and medium-voltage applications.
3. The study by Koura et al. (2010) highlights the history of multilevel converters over three decades and examines contemporary developments and industrial applications. It discusses modulation and new topologies.
4. An energy-balance control technique is presented by Chavarria et al. (2013) for a single-phase grid-connected H-bridge multilevel inverter that can integrate many separate PV arrays into the grid. In order to provide steady operation and effective power point tracking for every PV array, this method uses an energy-sampled data model and adapts to carrier pulse width modulation methods that are both phase-shifted and level-shifted. According to a survey of related literature, typical two- and three-level inverters are outperformed by seven-level inverters in terms of performance parameters.

III. PROPOSED SYSTEM

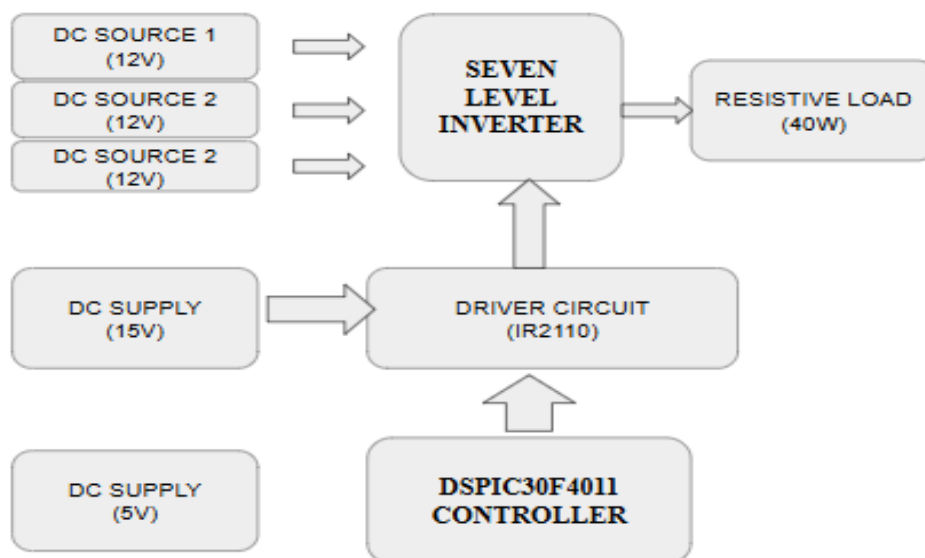


Figure 1: Block diagram of Proposed System

The proposed single-phase seven-level inverter is shown in Figure 1, offering the advantage of requiring fewer components while achieving higher output levels. The system utilizes a DSPIC30F4011 controller along with a driver circuit. Gating signals are produced using the Sinusoidal Pulse Width Modulation (SPWM) technique for the seven-level inverter. MOSFETs are used due to their several advantages, including high input impedance, suitability for medium-voltage applications, and low switching losses.

3.1 Working Principle of Seven Level Inverter

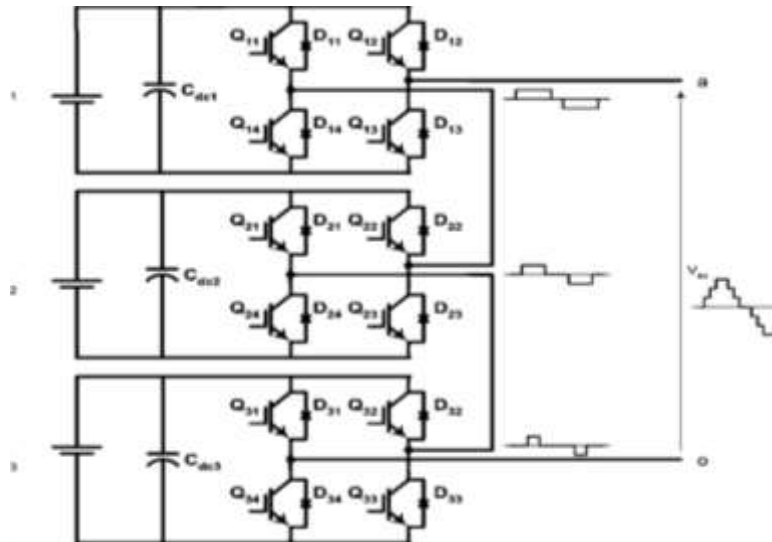


Figure 2: Circuit Diagram of seven Level Inverter

Figure 2 depicts the proposed seven-level inverter circuit. The circuit consists of two conversion stages: In the first stage, there are eight MOSFET switches labelled Q1 to Q8 and eight diodes D1 to D8, which help produce three different voltage levels. In the second stage, an H-bridge architecture incorporates eight MOSFET switches (Q1,Q2,Q3,Q4,Q5,Q6,Q7,Q8), enabling manufacturers to set the inverter level-shifting circuits and sub-interval sources on/off to achieve seven voltage levels at the inverter switching devices, as depicted in the accompanying table. Each operational mode is represented by links of effective elements. The switching pattern table is provided in Table 1

Table 1: Switching Pattern

Q1	Q2	Q3	Q4	Q5	Q6	Q7	Q8	Output Voltage
1	0	1	0	1	0	1	1	+3V
1	0	0	1	1	0	1	1	+2V
1	0	0	1	0	1	1	1	+V
0	0	1	1	1	0	1	1	0
0	1	1	0	0	1	1	1	-V
0	1	1	0	1	0	1	1	-2V
0	1	0	1	1	0	1	1	-3V

3.2 Method of Sinusoidal Pulse Width Modulation (SPWM)

Creation of Reference Signal: The first step in the SPWM process is to create a reference sinusoidal waveform, usually at the appropriate frequency and amplitude. The desired output voltage waveform that the inverter is trying to produce is represented by this reference signal.

Carrier Signal Generation: The high-frequency saw tooth serves as the carrier signal or triangle waveform. In our simulation frequency of the carrier wave is 5 KHz.

Comparison: A comparator is used to compare the carrier signal and the reference sinusoidal waveform. The instantaneous amplitude of the reference sinusoidal waveform is compared to the amplitude of the carrier signal at each point in time.

Pulse Generation: The width of the rectangular pulses is calculated based on the comparison result. The output pulse is set to its maximum width (100% duty cycle) when the amplitude of the carrier signal exceeds the amplitude of the reference sinusoidal waveform. On the other hand, the output pulse width is decreased in proportion to the carrier signal's amplitude if it is smaller than the reference sinusoidal waveform's amplitude.

Switching Control: The output pulses in the inverter's output stage control how power semiconductor devices (MOSFETs) switch on and off. These devices give an output voltage by regulating the pulse width waveform that closely resembles the shape of the reference sinusoidal waveform.

Low-Pass Filtering: To eliminate the high-frequency components and smooth out the resulting modulated waveform, which is made up of several pulses with different widths, the waveform is run through a low-pass filter. The desirable features of a sinusoidal waveform are closely resembled by the filtered output.

By adjusting the output voltage's amplitude and frequency, SPWM allows precise control the pulse width in proportion to the amplitude of the reference sinusoidal waveform [7]. This method makes high-quality AC output voltage with low harmonic distortion possible for inverters and other power conversion systems, which makes it appropriate for a variety of applications needing reliable and effective power conversion.

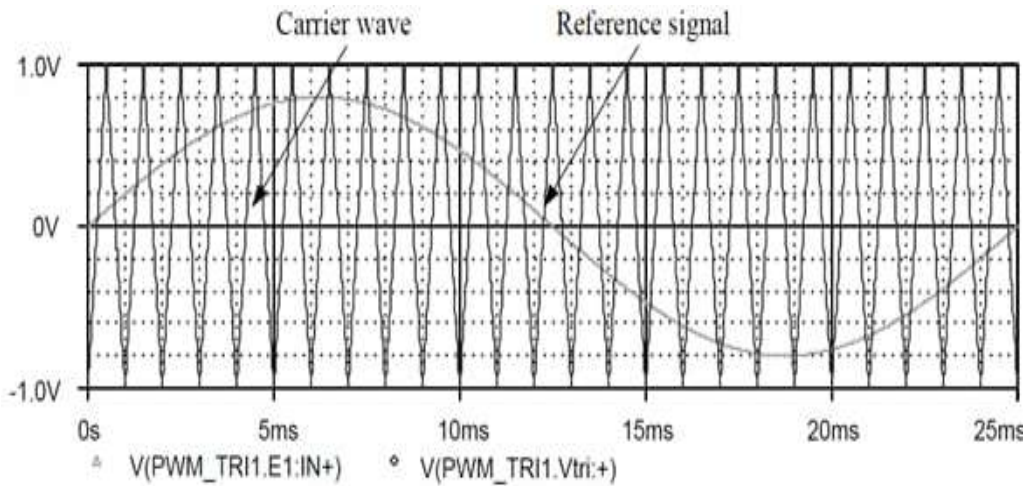


Figure 3: Sinusoidal Pulse width Modulation Method

IV. RESULTS AND DISCUSSION

4.1 SIMULATION CIRCUIT:

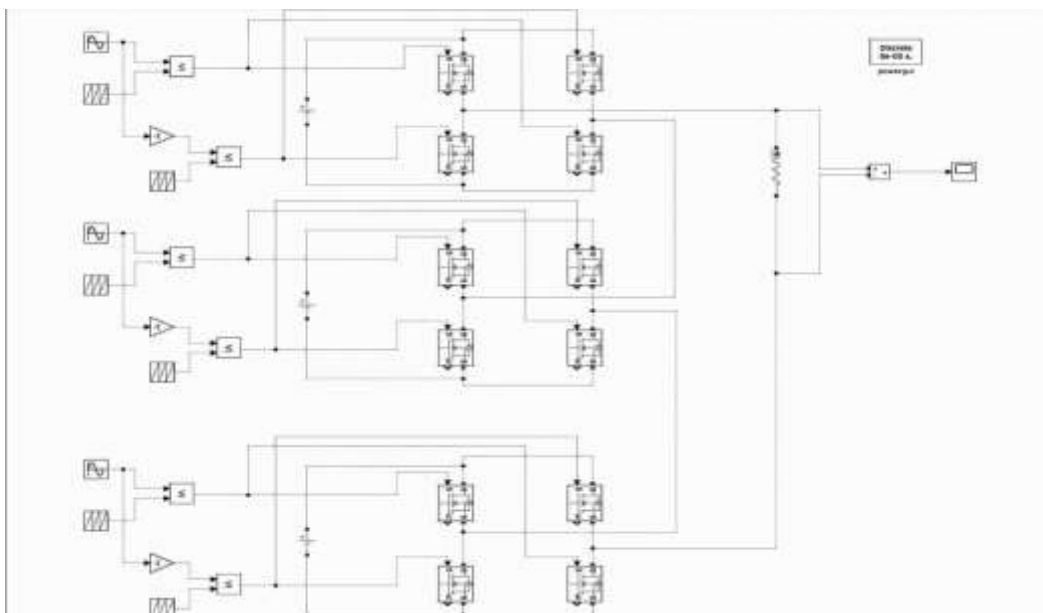


Figure 4:

4.2 SIMULATION OUTPUT:

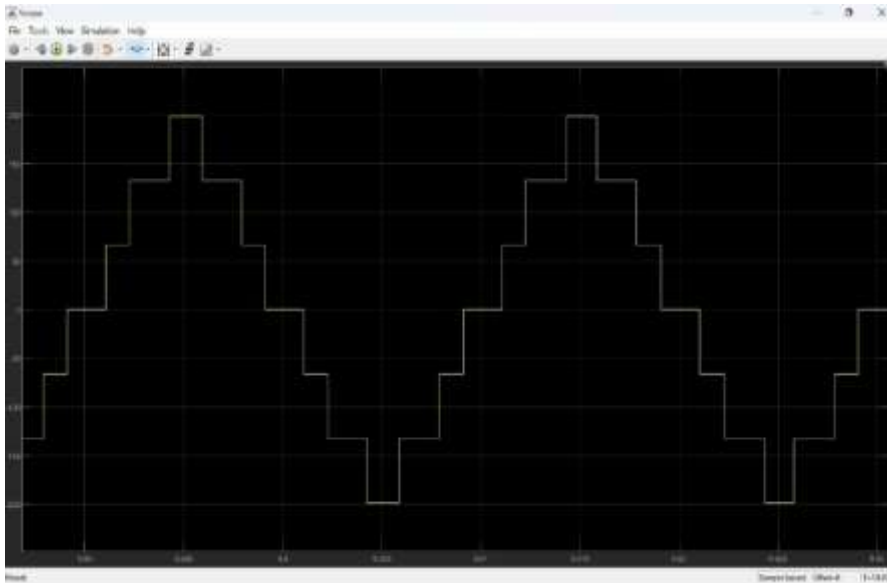


Figure 5:

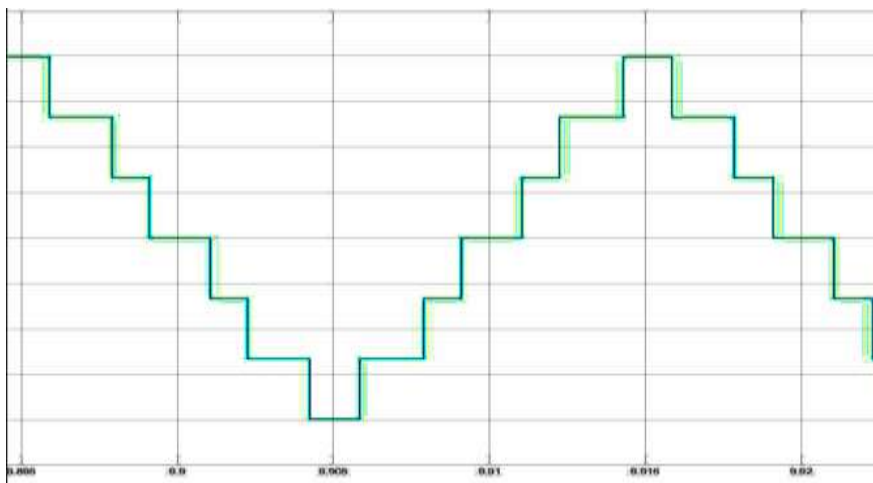


Figure 6:

V. CONCLUSION

The constructed and simulated single-phase seven-level inverter was tested for performance metrics such as Total Harmonic Distortion (THD) and reactive power. The simulation results show a THD value of 15%, which is within the restrictions set by IEEE Standard 519. The seven-level inverter was driven by gate pulses produced using the SPWM method. The efficiency of the seven-level inverter outperforms that of the ordinary two-level inverter.

VI. REFERENCES

- [1] Correa, P., Rodríguez, J., Pacas, M., & Villanueva, E. (2009). Control of a grid-connected solar system using a single-phase cascaded H-bridge multilevel inverter. *IEEE Industrial Electronics Transactions*, 56(11), 4399–4406.
- [2] Rodriguez, J., Malinowski, M., Gopakumar, K., & Perez, M. A. (2010). An analysis of multilayer inverters with cascades. *IEEE Industrial Electronics Transactions*, 57(7), 2197–2206.
- [3] Jamaludin, Jafferi. "Design and Implementation of a New Multilevel Inverter Topology with Share Power Switches", University of Malaya (Malaysia), 2023.
- [4] Debatosh Guha, Badal Chakraborty, Himadri Sekhar Dutta. "Computer, Communication and Electrical Technology", CRC Press, 2017.