e-ISSN: 2582-5208
International Research Journal of Modernization in Engineering Technology and Science
(Peer-Reviewed, Open Access, Fully Refereed International Journal)
Volume:06/Issue:11/November-2024 Impact Factor- 8.187 www.irjmets.com

OPTIMIZED DESIGN OF MIXED LOGIC LINE DECODERS FOR LOW POWER AND HIGH SPEED

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ABSTRACT

Since integrated circuits were invented, consumer demand has focused on devices that are powerful, energy-efficient, small, and affordable. This demand has driven the development of increasingly refined sub-micron technologies, such as 32nm, 22nm, and 14nm. A detailed review of technology aspects for low-power applications is conducted, with an evaluation of emerging technologies in terms of power, performance, and area. We aim to design 2-4 decoders using a mixed-logic approach. Mixed logic, a gate-level design strategy, allows digital circuit designers to separate circuit functionality from its physical form, producing logic expressions and diagrams that match. For the 2-4 decoder, two topologies are proposed: a 14-transistor design for lower transistor count and power dissipation, and a 15-transistor design for optimal power-delay performance. Normal and inverting decoders are implemented in both cases, creating four designs. Each has full-swing capability and a reduced transistor count versus CMOS. Comparative SPICE simulations show the proposed designs generally achieve better power and delay performance, often outperforming CMOS.

Keywords: Decoder, Complementary Pass Transistor Logic (CPL), NOR Gate, AND Gate, NAND Gate, OR Gate, CMOS.

I. INTRODUCTION

Digital systems represent discrete information through binary codes, where an n-bit binary code can define up to 2^n unique elements. A decoder is a combinational circuit that converts binary data from n input lines to a maximum of 2^n distinct outputs, or fewer if some binary combinations are not used. The circuits explored here are n-to-m line decoders, designed to generate $m=2^n$ minters based on the n input variables.

Static CMOS circuits dominate in integrated circuit logic gate design. They use complementary nMOS pull-down and pMOS pull-up networks, providing strong performance and resistance to noise and device variation. This complementary CMOS design offers robustness against voltage scaling and transistor sizing, ensuring reliable operation even at low voltages and smaller transistor sizes. Since input signals connect only to transistor gates, CMOS logic simplifies design complexity and supports efficient cell-based synthesis and design.

Pass transistor logic (PTL) emerged in the 1990s as an alternative to CMOS logic, with various design styles introduced to enhance speed, power efficiency, and area. The key distinction of PTL is that inputs are applied not only to the gates but also to the source and drain terminals of the transistors. PTL circuits are typically built using single nMOS or pMOS pass transistors, or by employing transmission gates, which consist of parallel pairs of nMOS and pMOS transistors.

The most commonly used design is the complementary CMOS full adder (C-CMOS), which follows a standard CMOS structure with pull-up and pull-down transistors, utilizing 28 transistors. Another standard adder is the Complementary Pass Transistor Logic (CPL) with swing restoration, which requires 32 transistors. CPL uses multiple intermediate nodes and their complements to generate the outputs. The key distinction between pass transistor logic and complementary CMOS logic lies in the fact that the pass logic network is connected to input signals at the source side, rather than to power lines. The Transmission Gate Full-Adder (TGA) design uses only 20 transistors, while the double pass transistor full adder, based on double pass transistor logic, utilizes 48 transistors and employs both NMOS and PMOS logic networks.

Electronic technology started with vacuum tubes as the primary active components in circuits, which were later replaced by semiconductor transistors. The growth of microelectronic technology, particularly in monolithic circuits, enables the combination of active and passive components on a single chip. High-speed serializers/deserializers (SerDes) are now being widely used in communication systems to facilitate serial

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interconnections

II. PROPOSED SYSTEM

In Transmission Gate Logic (TGL), AND/OR gates can be implemented efficiently, making them useful for line decoder applications. The 2-input TGL AND/OR gates, illustrated in Fig. 1(a) and (b), offer full swing operation but are not restoring under all input conditions. For Pass Transistor Logic (PTL), two major circuit styles exist: nMOS-only designs, like Complementary Pass-Transistor Logic (CPL), and mixed nMOS and pMOS transistor designs, like Double Pass-transistor Logic (DPL) and Dual Value Logic (DVL). Here, we focus on DVL, which maintains the full swing of DPL while reducing transistor count. The 2-input DVL AND/OR gates, shown in Fig.1(c) and (d), are also full swing but non-restoring.

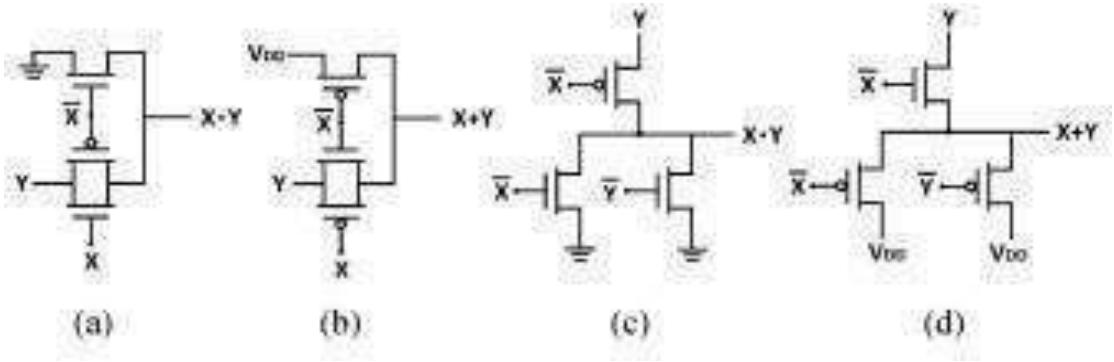

Figure 1: Three-transistor AND/OR gates considered in this work. (a) TGL AND gate. (b) TGL OR gate. (c) DVL ANDgate. (d) DVL OR gate.

TGL and DVL gates, given complementary inputs, can function with only three transistors. Since decoders are high fan-out circuits, a few inverters can serve multiple gates, allowing TGL and DVL designs to reduce the number of transistors required. An important shared trait is these gates' asymmetrical design, meaning their input loads are not balanced. As indicated in Fig.1, inputs X and Y are used for these gates. In TGL setups, input X drives all three transistor gate terminals, while Y is passed to the output node via the transmission gate. In DVL configurations, input X manages two gate terminals, while Y influences one and transfers through a pass transistor to the output..

We will refer to X and Y as the control signal and propagate signal of the gate, respectively.

Using a complementary input as the propagate signal is not a good practice, since the inverter added to the propagation path increases delay significantly. Therefore, when implementing the inhibition (A B) or implication (A + B) function, it is more efficient to choose the inverted variable as control signal. When implementing the AND (AB) or OR (A + B) function, either choice is equally efficient. Finally, when implementing the NAND (A + B) or NOR (A B) function, either choice results to a complementary propagate signal, perforce.

14-Transistor 2–4 Low-Power Topology

A 2–4 line decoder typically requires 16 transistors when designed with either Transmission Gate Logic (TGL) or Dynamic Voltage Logic (DVL) gates, allocating 12 transistors for AND/OR gates and 4 for inverters. However, by combining both gate types and arranging signals strategically, one inverter can be removed, reducing the transistor count to 14. In this optimized setup, we eliminate the B inverter by using a mix of TGL and DVL gates where the complementary B signal is no longer necessary. For example, the Do minterm (A B) is implemented using a DVL gate with A as the propagate signal, while D1 (AB) is implemented using a TGL gate with B as the propagate signal. D2 and D3 follow similar configurations with DVL and TGL gates, respectively, using either A or B as the propagate signal. This configuration saves power, reduces transistor count, and minimizes switching activity. A similar approach applies to a 2–4 inverting decoder using OR gates, yielding a 14-transistor circuit with 5 nMOS and 9 pMOS transistors. By again eliminating the B inverter, a streamlined design is achieved, with I0 and I2 implemented using TGL and I1 and I3 with DVL. These designs are termed “2-4LP” for low power and “2-4LPI” for inverting, resulting in simplified, efficient topologies with lower logical effort and reduced power dissipation. Their schematics are shown in Fig.2(a) and (b), respectively.

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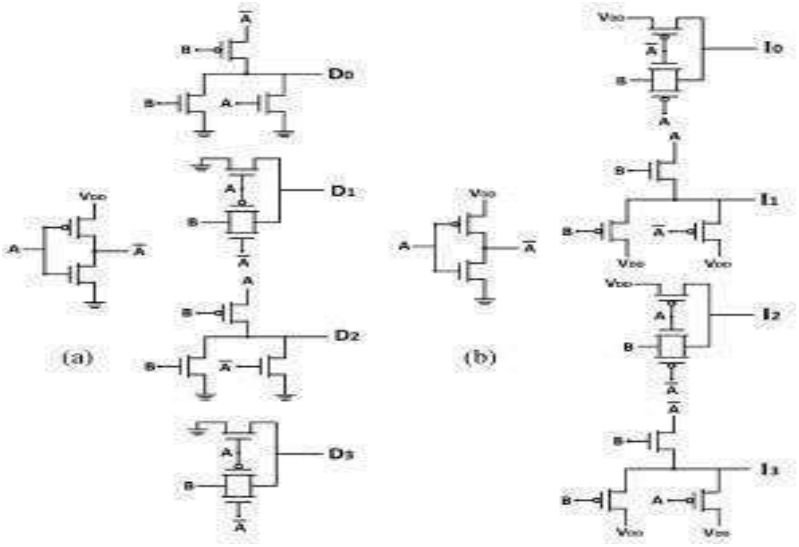

Figure 2: New 14-transistor 2–4 line decoders. (a) 2–4 LP. (b) 2–4 LPI.

15-Transistor 2–4 High-Performance Topology

The low-power designs described have a trade-off in terms of worst-case delay, which results from using the complementary A signal as the propagate signal in D0 and I3. However, D0 and I3 can be implemented more effectively with static CMOS gates, without relying on complementary signals. For instance, implementing D0 with a CMOS NOR gate and I3 with a CMOS NAND gate only adds one transistor per topology. These new 15-transistor (15T) designs, named "2–4HP" (9 nMOS, 6 pMOS) and "2–4HPI" (6 nMOS, 9 pMOS), improve delay significantly with only a minimal increase in power dissipation. In these names, "HP" denotes high performance, and "I" denotes inverting. Schematics are shown in Fig. 3(a) and (b), respectively

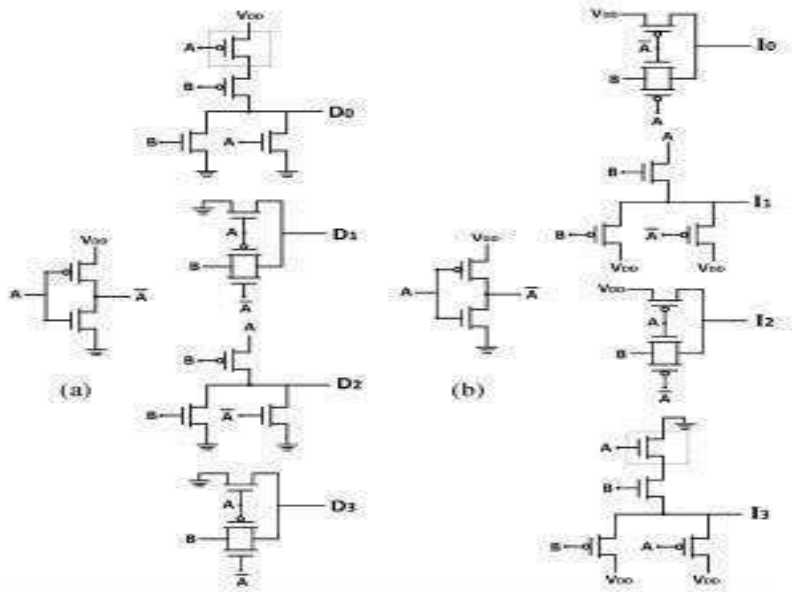

Figure 3: New 15-transistor 2–4 line decoders.(a) 2–4HP. (b) 2–4HPI.

III. SIMULATION AND RESULT

The proposed designs were compared to their conventional counterparts: 2–4LP and 2–4HP with the 20T, and 2–4LPI and 2–4HPI with the inverting 20T. Results show that 2–4LP offers a 9.3% reduction in power dissipation over CMOS 20T, though with a trade-off of 26.7% higher delay and a 15.7% increase in PDP. Conversely, 2–4HP outperforms CMOS 20T in every category, achieving reductions in power by 8.2%, delay by 4.3%, and PDP by 15.7%. Both inverting designs, 2–4LPI and 2–4HPI, also surpass the inverting CMOS 20T across all metrics, with 2–4LPI demonstrating significant enhancements.

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power, delay, and PDP by 13.3%, 11%, and 25% respectively, while 2–4HPI does so by 11.2%, 13.2%, and 25.7%.

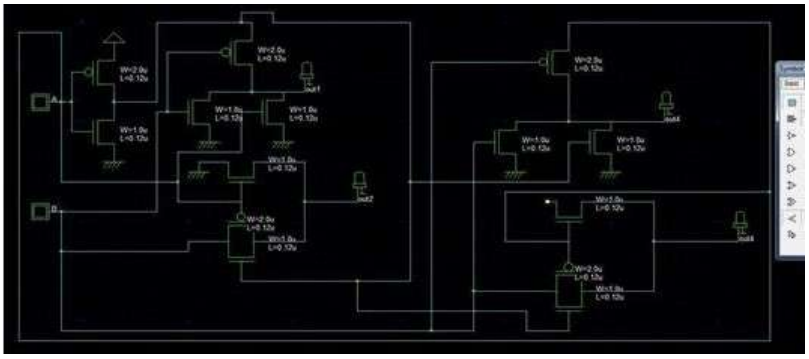

Figure 4 {a}: Architecture

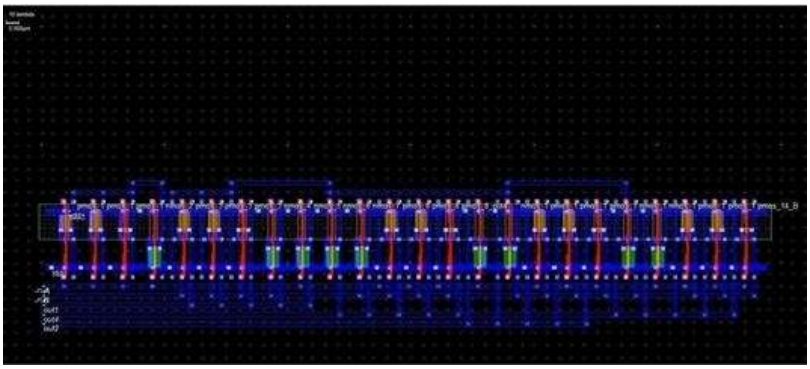

Figure 4 {b}: layout diagram.

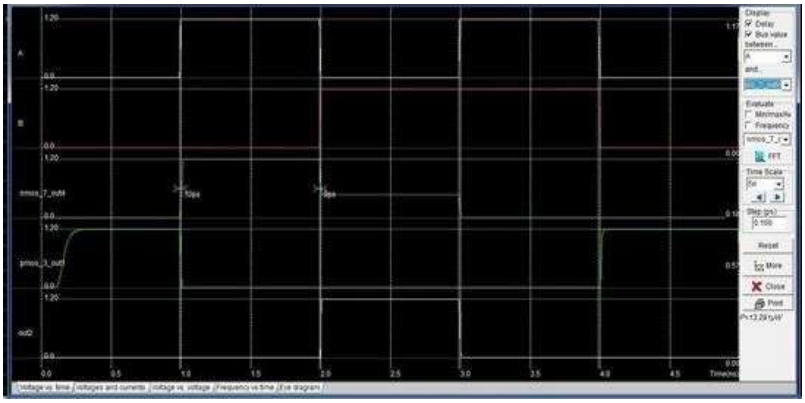

Figure 4 {c}: Waveforms

Figure 4: Output for 2-4 LP line decoder (14 Transistor).

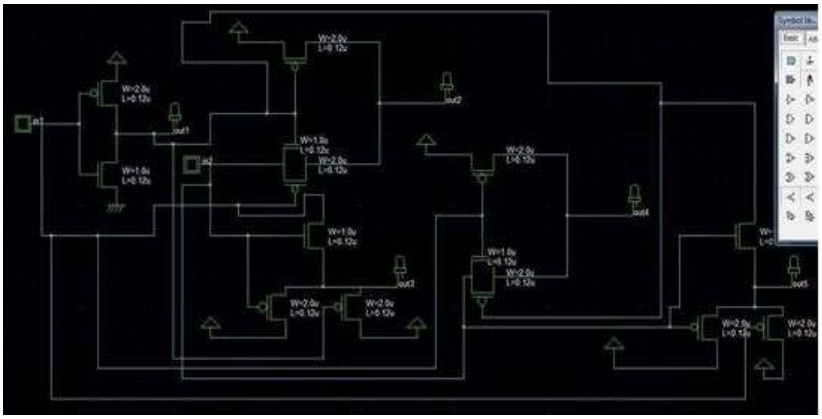

Figure 5 {a}: Architecture.

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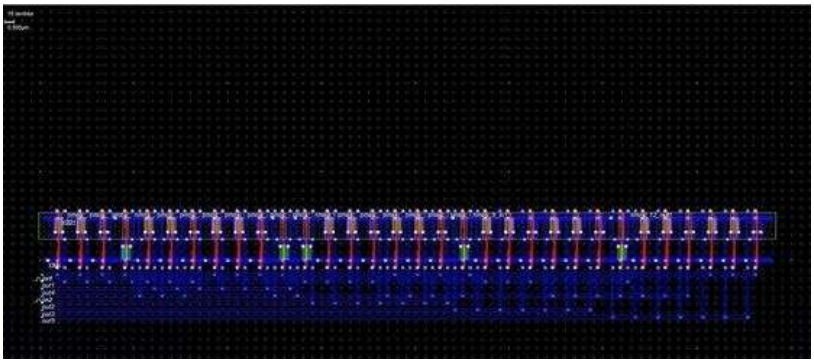

Figure 5 {b}: Layout diagram

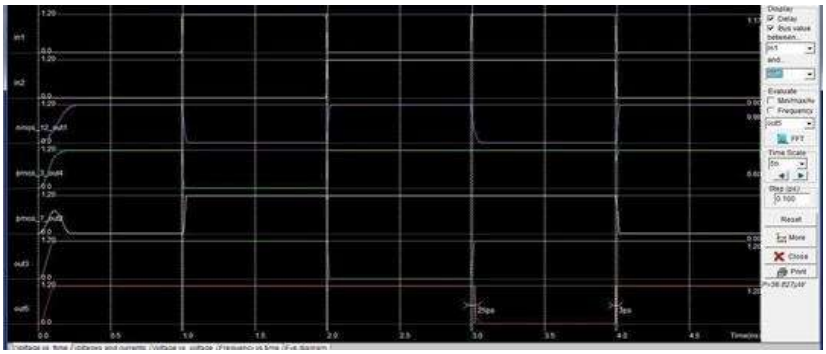

Figure 5 {c}: Waveforms.

Figure 5: The output for 2-4 LPI line decoder (14 Transistor).

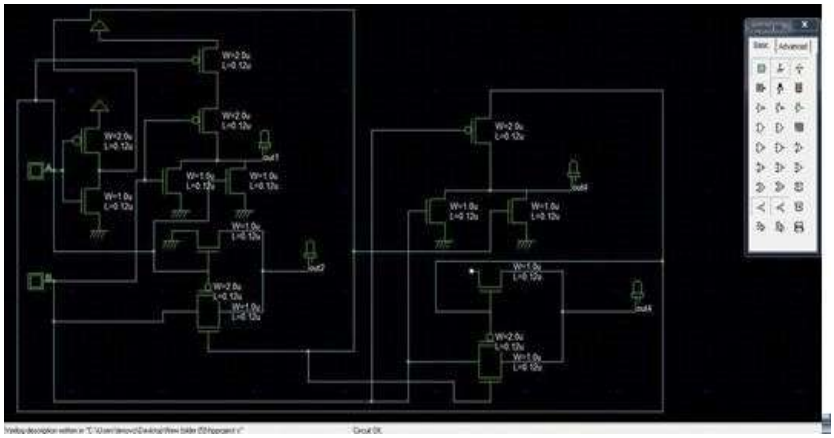

Figure 6 {a}: Architecture

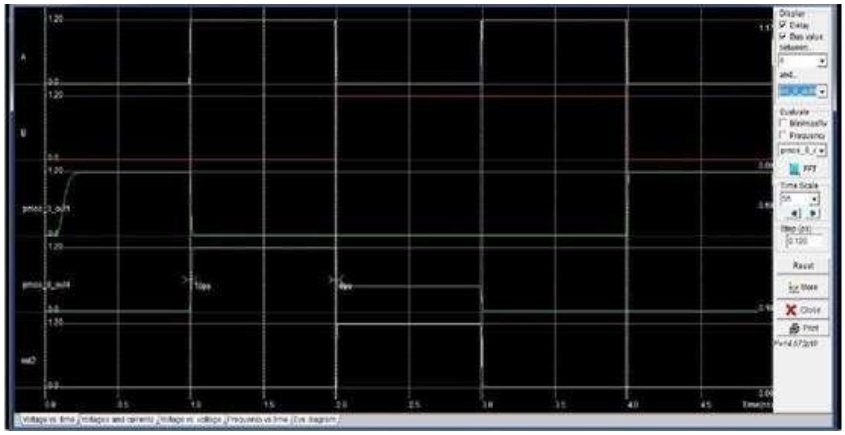

Figure 6{b}: Waveforms.

Figure 6: The output for HP line decoder (15 Transistors).

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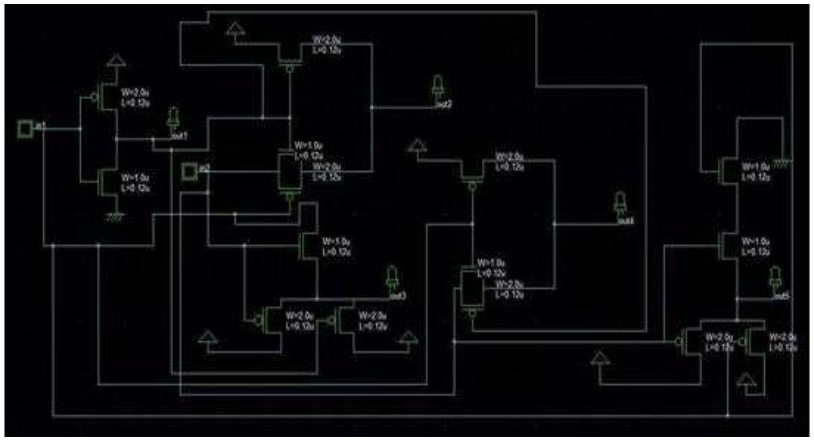

Figure 7{a}: Architecture

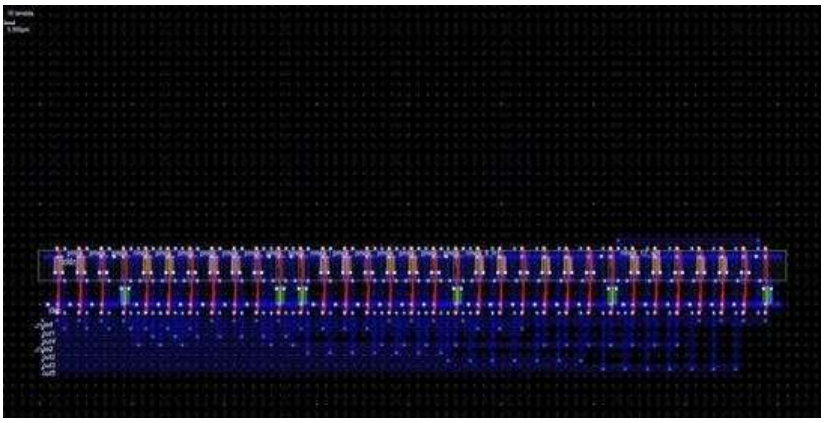

Figure 7{b}: Layout diagram.

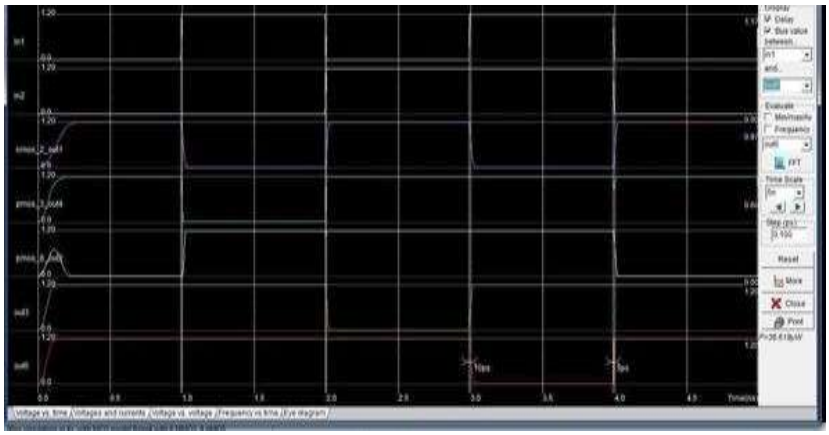

Figure 7: Output for 2-4 HPI Line decoder (15 Transistors). .

IV. CONCLUSION

In this brief, we propose an effective mixed logic design strategy for decoder circuits, integrating TGL, DVL, and static CMOS. This approach has led to the creation of four new 2–4 line decoder layouts—2–4LP, 2–4LPI, 2–4HP, and 2–4HPI—that offer lower transistor counts and enhanced power-delay performance compared to conventional CMOS decoders. Comparative simulations at 32 nm confirm the superiority of these designs. The 2–4LP layout is especially suited for applications that prioritize area and power minimization. The 2–4LPI, 2–4HP, and 2–4HPI configurations, along with their larger 4–16 counterparts (4–16LP, 4–16HPI, and 4–16HP), offer efficient, well-rounded solutions that can serve as building blocks for larger decoders, multiplexers, and other combinational circuits with varying performance requirements. With reduced transistor counts and low power features, these designs benefit both bulk CMOS and SOI processes. Furthermore, the circuits are implemented at the layout level, making them ideal for standard cell libraries and RTL design.

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